

Compal Confidential

Model Name : SAGE 3G
Compal Project Name : V1JB1
File Name : LA-A041P

Compal Confidential

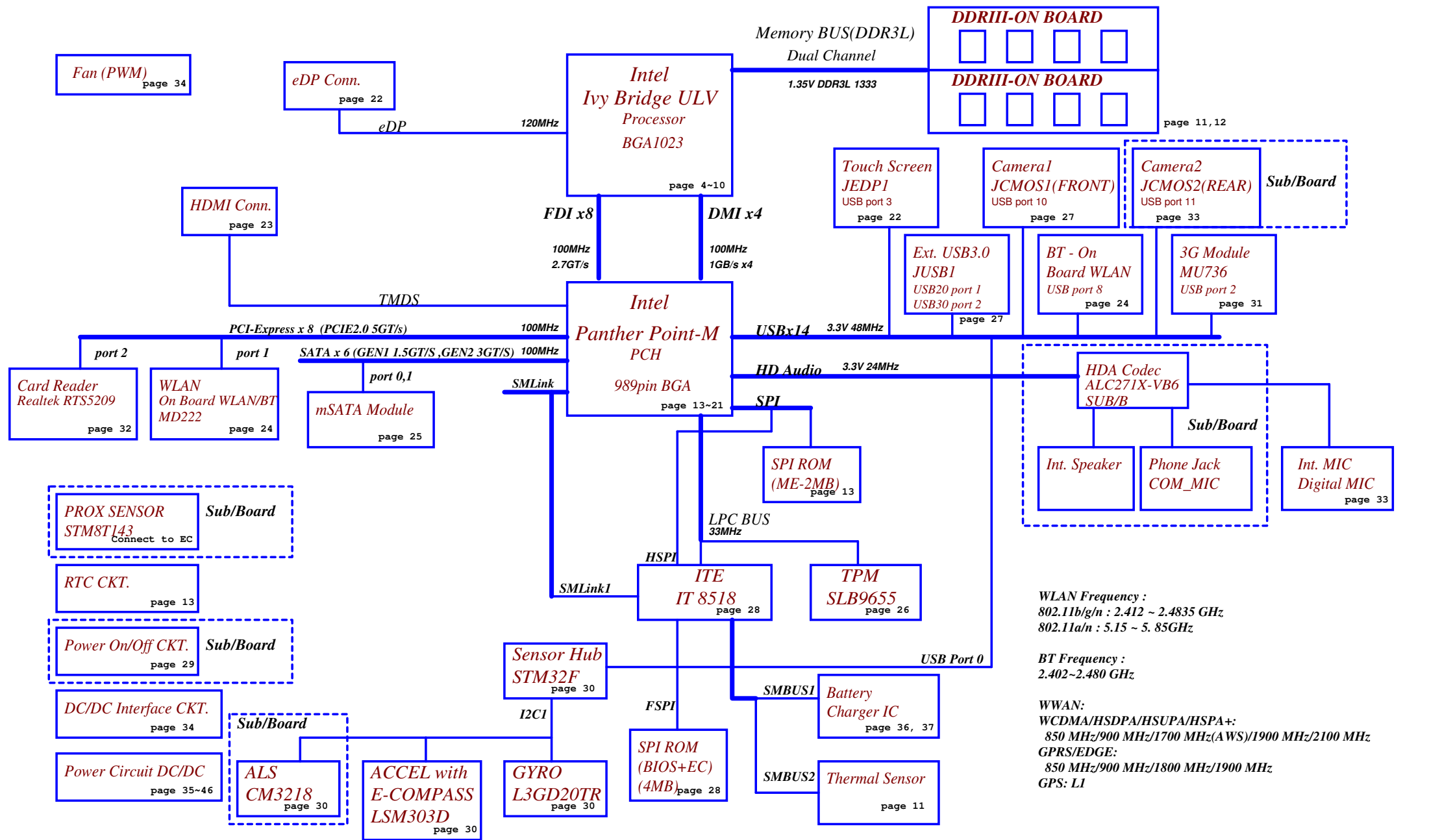
V1JB1 UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor
/Panther Point 989p PCH
/ DDR3L Memory Down *8

2013-03-26

REV : 2 . 0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	Cover Page
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				V1JB1 M/B LA-A041P Schematic	2.0
				Date: Tuesday, March 26, 2013	Sheet 1 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Block Diagrams	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				V1J1B1 M/B LA-A041P Schematic	0.1
				Date: Tuesday, March 26, 2013	Sheet 2 of 52

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+V5REF_SUS	+5VALW to +V5REF_SUS power rail for PCH	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device	Address
ChannelA	A0 1010 000X
ChannelB	A4 1010 010X

BOM Config

Sensors List

Connect to	Function	Device
Sensor Hub	Gyroscope	ST - L3GD20TR
Sensor Hub	Accel+E-Compass	ST - LSM303DLHCTR
PCH (USB P3)	Sensor Hub	ST - STM32F103RCY6TR
Sensor Hub	ALS	Capella - CM3218
EC	Prox	ST-STM8T143AU62TTRC06

EC SM Bus2 address

Device	Address
--------	---------

Sensor HUB SM Bus address

Device	Address
Gyroscope	D1 1101 000X b
	D3 1101 001X b
E-compass + G sensor	33 0011 001X b
ALS sensor	21 0010 000X b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	2.0*
5	
6	
7	

Note :

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	Sensor Hub
		1	Ext. USB Connector
		2	3G Module - MU736/ME906
		3	Touch Screen
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Bluetooth(WLAN Module)
		9	Debug Port(Reserve)
	UHCI3	10	Camera(Front)
		11	Camera(Rear)
		12	
		13	

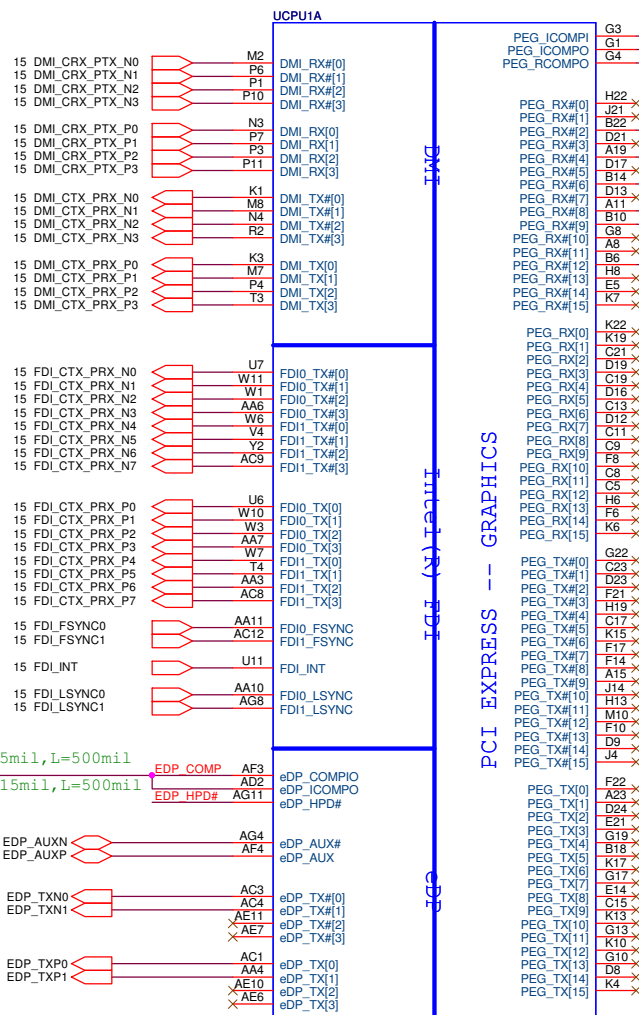
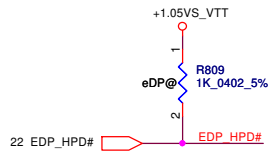
BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
Dual Channel DDR	128@
eDP	eDP@
PCH	HM77@
Normal S3	S3@
Deep S3	DS3@
TPM	TPM@
Non TPM SKU	WOTPM@
Hall Sensor	LID@
Foxconn MD222	FOXMD222@
Lite-On MD222	LIONMD222@
For EMI/RF (Pop)	EMC@
For EMI/RF (Unpop)	XEMC@
Sensor (Intel F/W)	INTEL@
Sensor (ST F/W)	ST@
3G SKU	3G@
3G SKU (EMC part)	3GEMC@

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Notes List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				V1JBI M/B LA-A041P Schematic	0.1
				Date: Wednesday, March 13, 2013	Sheet 3 of 52

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms, even if disable eDP function...

Add eDP circuit



UMA only=>PEG NC

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms

PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

G3, W=4mil, S=15mil, L=500mil
G1, W=12mil, S=15mil, L=500mil
G4, W=4mil, S=15mil, L=500mil

SAGE 3G PVT
For DFB demand

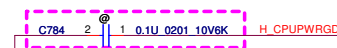
IVY-BRIDGE_BGA1023
IVB@

CPU P/N:
1.I3-3217 SA00005L5C0:S IC AV8063801058401 SR0N9 L1 1.8G ABO!
2.I5-3317 SA00005K6B0:S IC AV8063801058002 SR0N8 L1 1.7G ABO!
3.I3-2365 SA000051H60:S IC AV8062701047904 SR0CV J1 1.4G ABO!

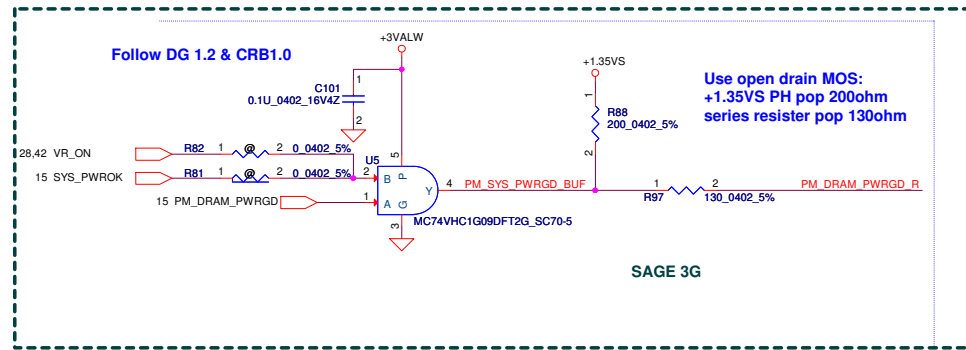
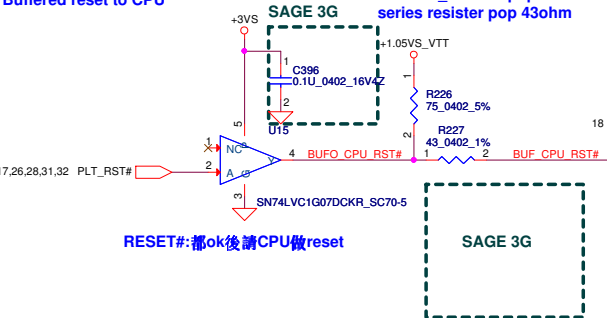
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2011/06/24	Deciphered Date	2012/06/02	PROCESSOR(1/7) DMI,FDI,PEG	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Title	
					Size	
					Document Number	
					Rev	
					0.1	
					Date: Wednesday, March 13, 2013	
					Sheet 4 of 52	
					V1JB1 M/B LA-A041P Schematic	

PCH->CPU
UNCOREPWROK:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.2 & CRB1.0



Follow DG 1.2 & CRB1.0
Buffered reset to CPU



PROC_SELECT#
Future platforms,PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

Processor Pullups follow CRB1.0

Use open drain MOS:
+1.05VS_VTT PH pop 75ohm
series resistor pop 43ohm

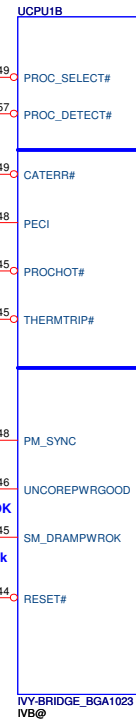
SAGE 3G

UNCOREPWROK:除了CPU_CORE以外的電OK

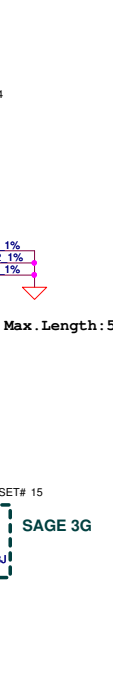
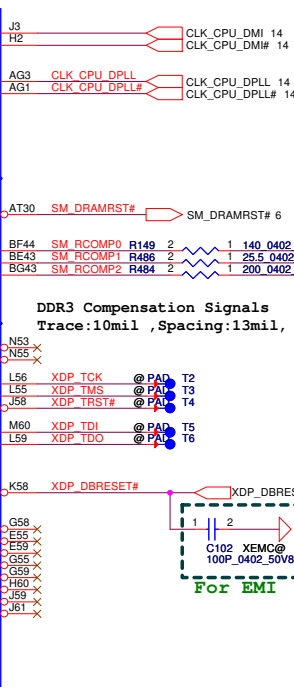
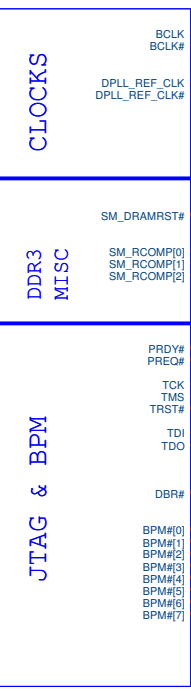
SM_DRAMPWROK:DRAM power ok

Use open drain MOS:
+1.35VS PH pop 200ohm
series resistor pop 130ohm

SAGE 3G



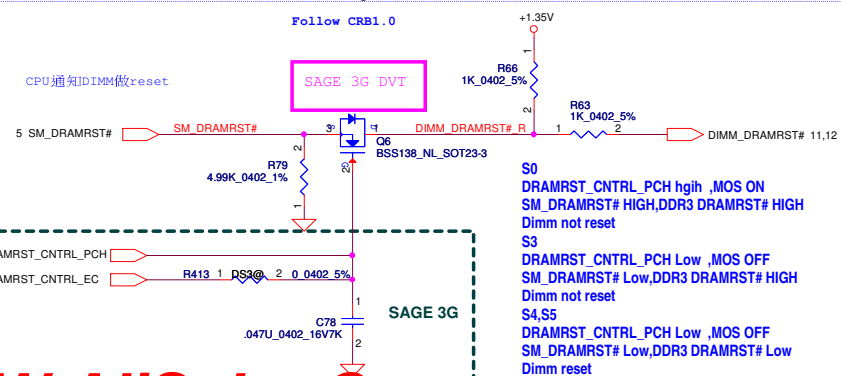
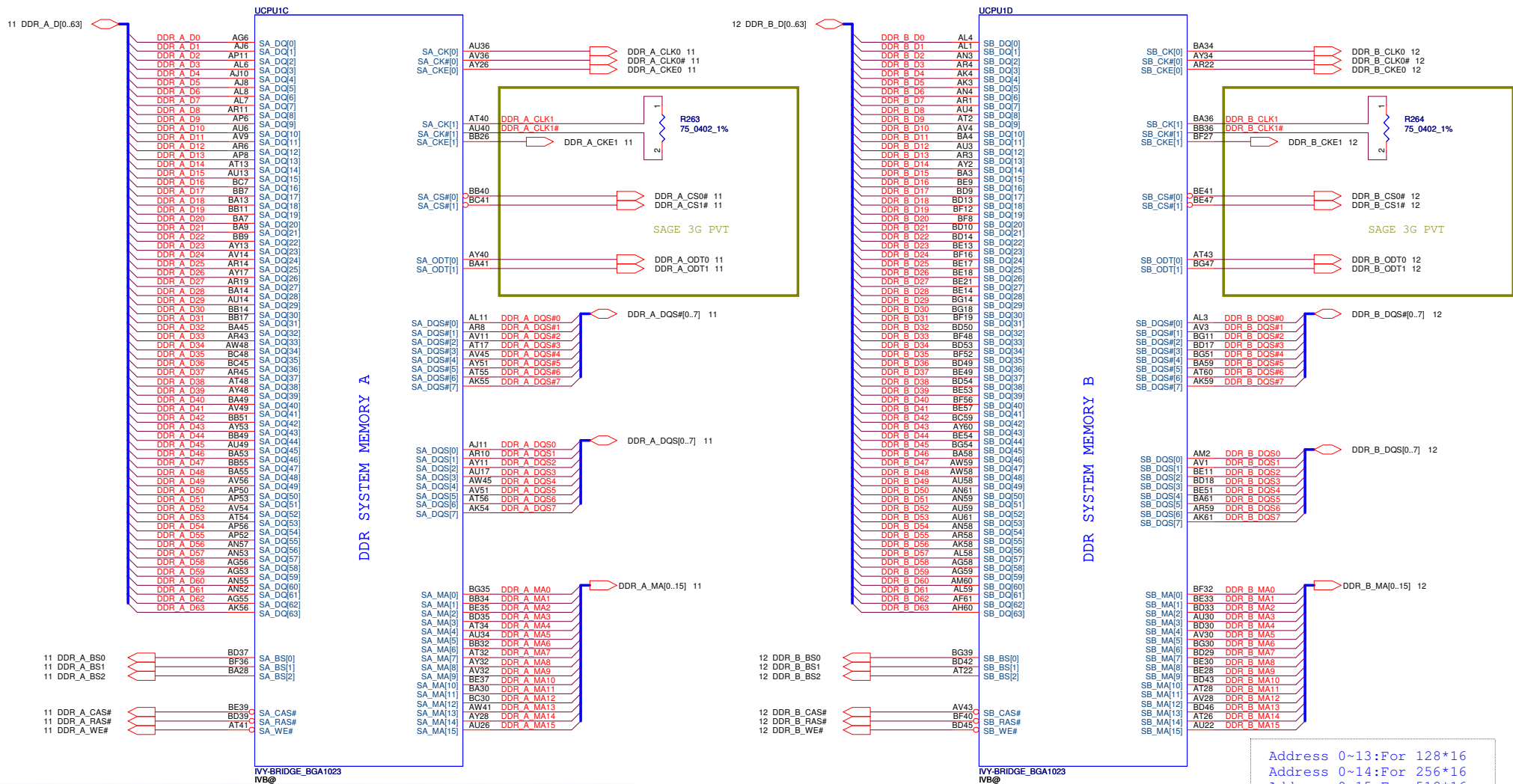
MISC
THERMAL
PMR MANAGEMENT
JTAG & BPM



CLK_CPU_DPLL# R116 2 @ 1 1K 0402 5%
CLK_CPU_DPLL R117 2 @ 1 1K 0402 5%
Checklist1.0 P.64 Processor Graphis Disable Guide
DIS only SKU or UMA eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

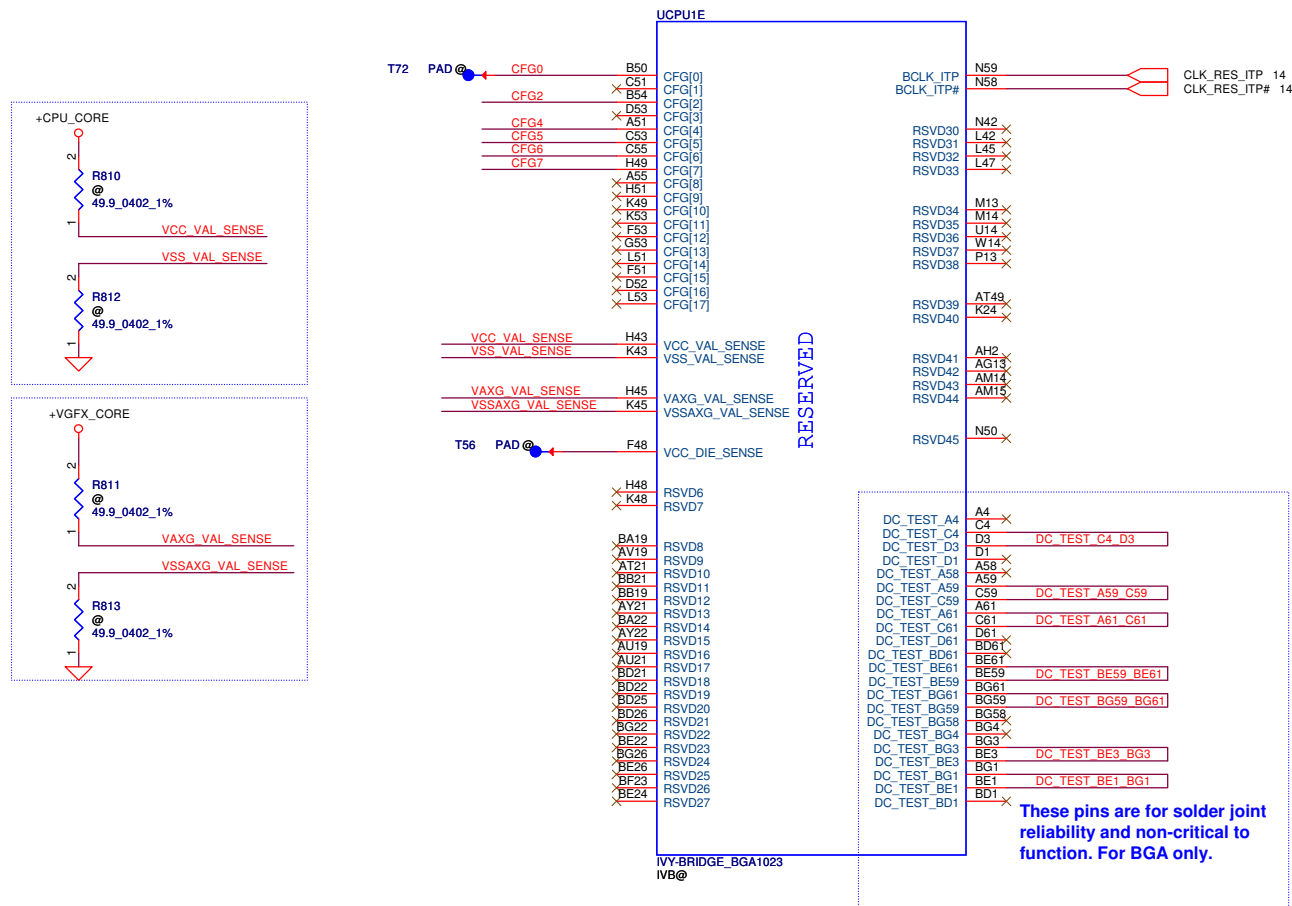
XDP_DBRESET# R569 2 @ 1 1K 0402 5%
CRB1.0 PH 1K +3VS
Check list 1.0 PH 5K +3VS
Check list 1.2 PH 10K +3VS
Debug port DG1.1-1.2 50-5K ohm

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	PROCESSOR(2/7) PM,XDP,CLK	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				V1JBI M/B LA-A041P Schematic	0.1
				Wednesday, March 13, 2013	Sheet 5 of 52



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/24				Deciphered Date			
2011/06/24				2012/06/02				Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number				Revision			
2011/06/24				2012/06/02				VIJBI M/B LA-A041P Schematic			
Date: Wednesday, March 13, 2013				Sheet 6 of 52				Rev 0.1			

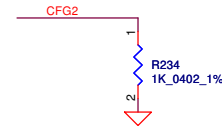
WWW.AliSaler.Com



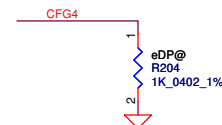
Default "1",EDS R1.0 P.88

CFG Straps for Processor

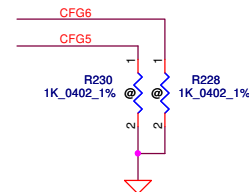
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0:Lane Reversed



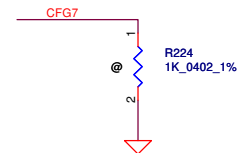
eDP enable	
CFG4	★ 1:Disable 0:Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	★11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express

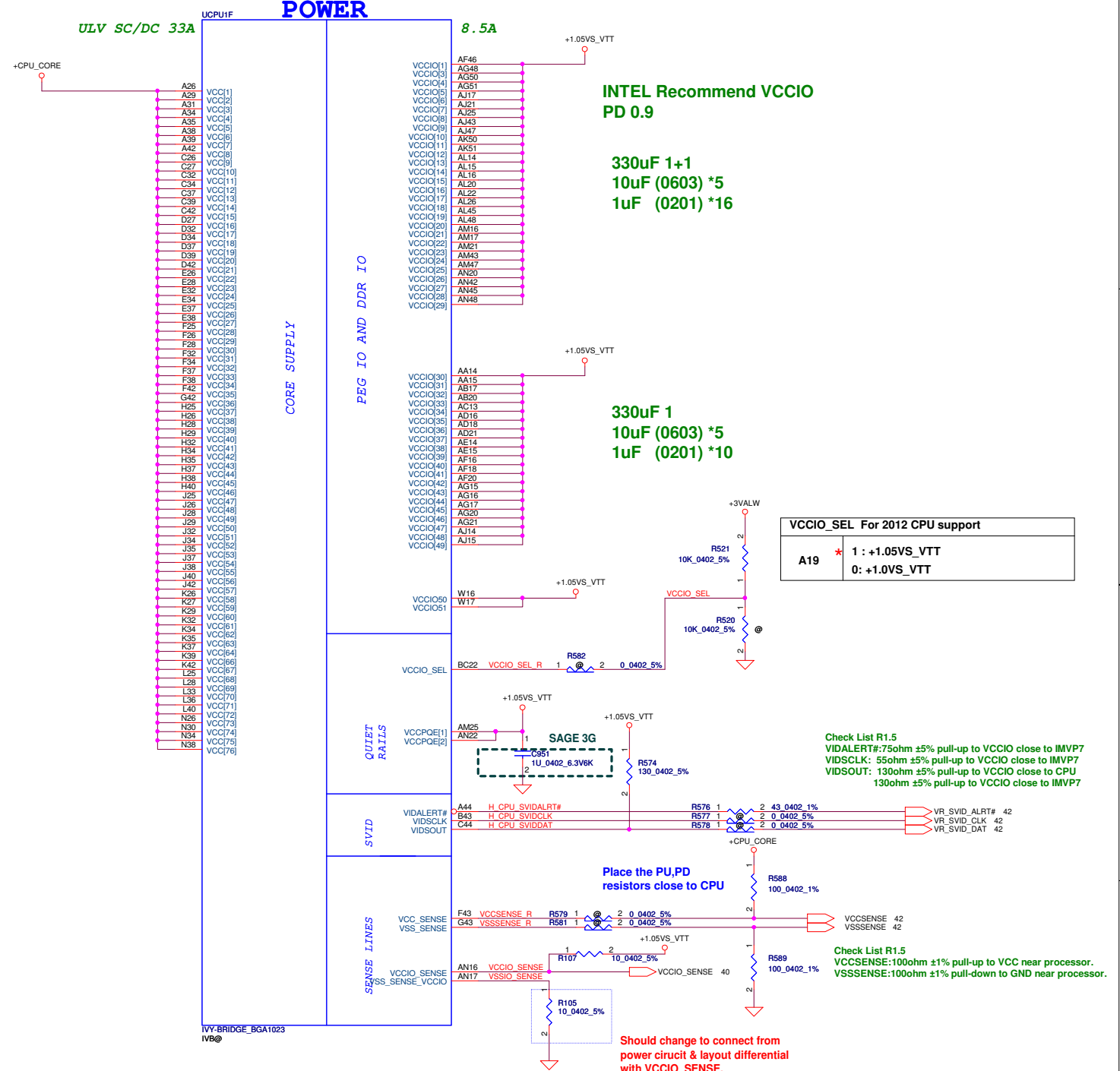


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title PROCESSOR(4/7) RSVD,CFG	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number V1J1B1 M/B LA-A041P Schematic
				Date: Wednesday, March 13, 2013	Rev 0.1
				Sheet 7	of 52

INTEL Recommend VCC
3*330uF,12*22uF(0805),16*2.2uF(0402)
PD0.9



Security Classification	Compal Secret Data			Compal Electronics, Inc. PROCESSOR(5/7) PWR,BYPASS		
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	V1JBI M/B LA-A041P Schematic	0.1
				Date:	Wednesday March 13 2013	Sheet 1 of 50

INTEL Recommend VAXG
2*330uF,5*22uF(0805),6*10uF(0603),6*1uF(0402)
PD 0.9

Check List R1.5
VCCAXG_SENSE:100ohm ±5% pull-up to VCC near processor.
VSSAXG_SENSE:100ohm ±5% pull-down to GND near processor.

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD 0.9

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.9

ULV SC/DC GT1: 18A
GT2: 33A

UCPU1G

POWER

GRAPHICS

DDR3 - 1.5V RAILS

QUIET RAILS

SA RAIL

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandy bridge not support M3,
Check list1.0 & CRB say can NC

+V_SM_VREF should
have 20 mil trace width

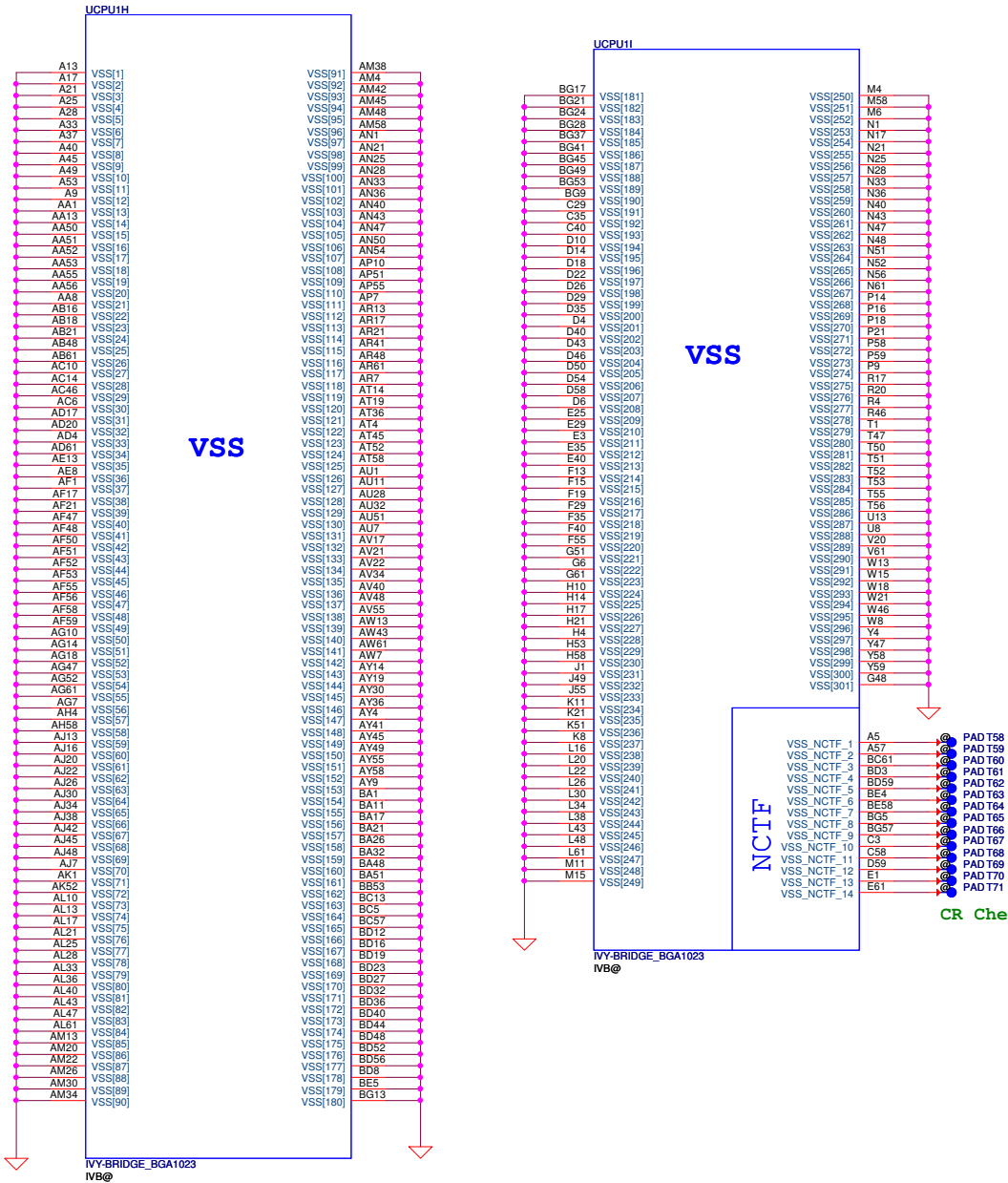
INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.9

Short for +1.35VS to +1.35V_CPU_VDDQ

Place BOT OUT Conn

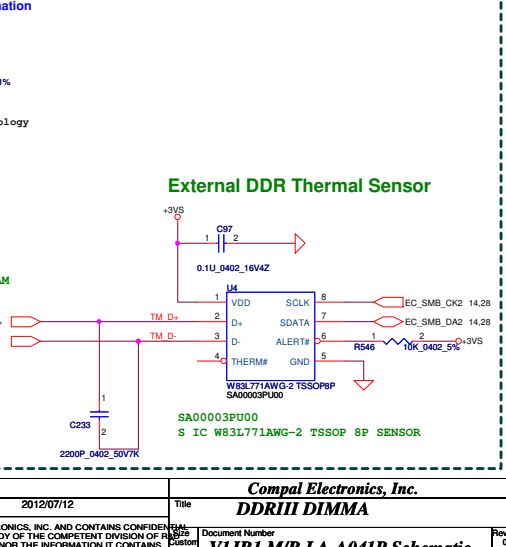
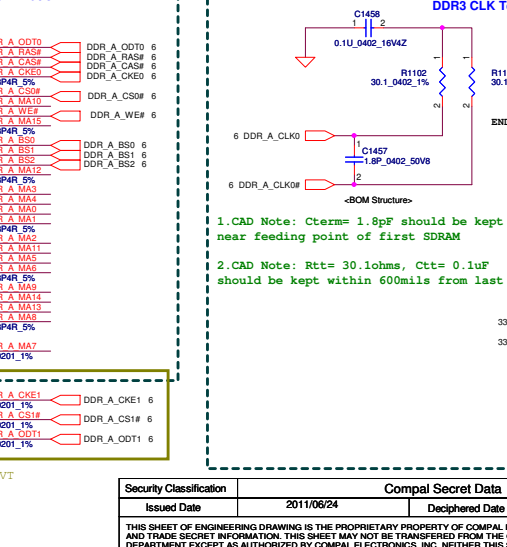
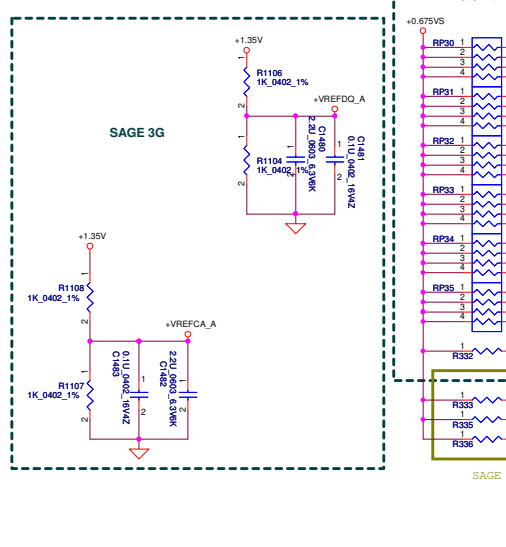
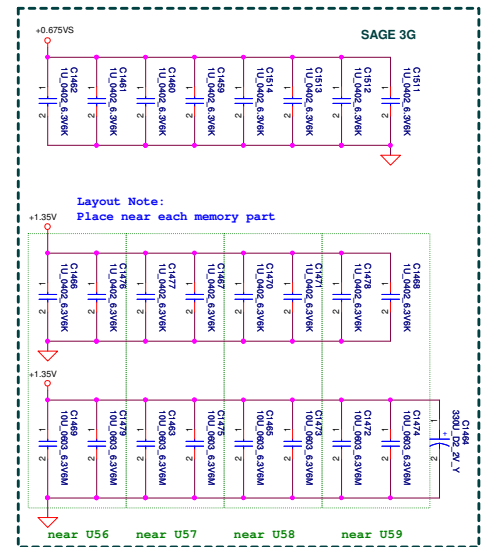
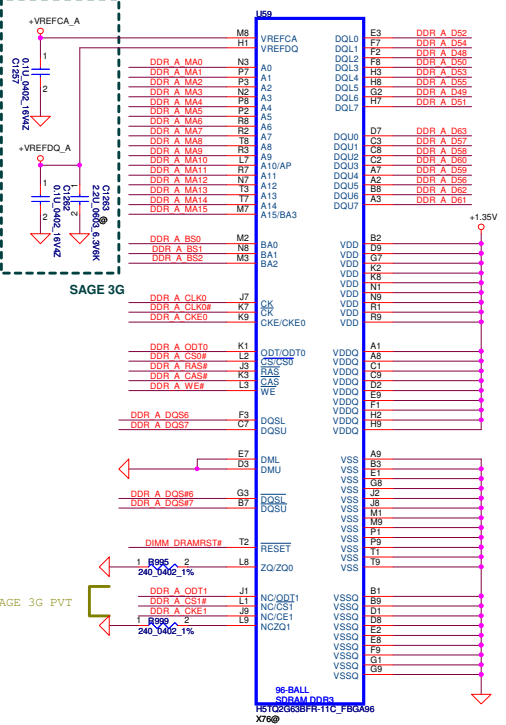
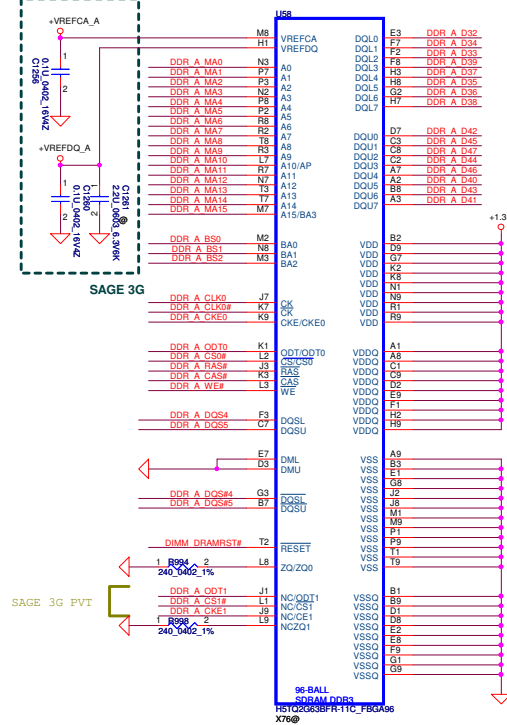
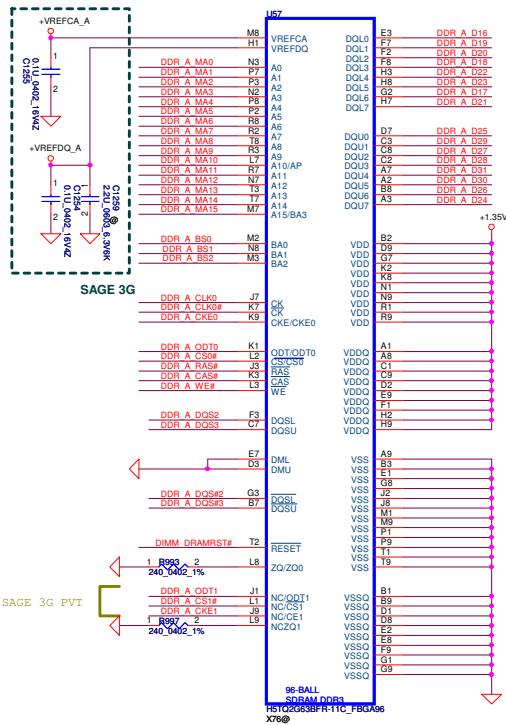
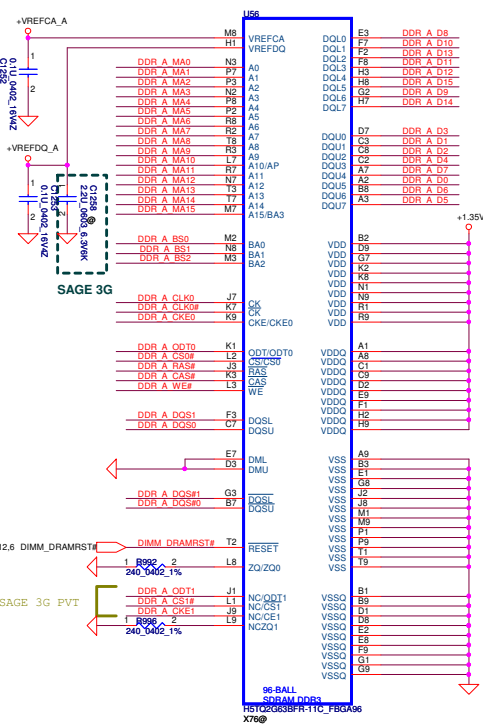
VCCSA_VID
For 2012 future CPU
VCCSA voltage select

VCCSA					
VID0	VID1	Vout	SNB	IVB	ULV
0	0	0.9V	V	V	V
0	1	0.8V	V	V	V
		0.85V			
1	0	0.725V	X	V	V
1	1	0.675V	X	V	V



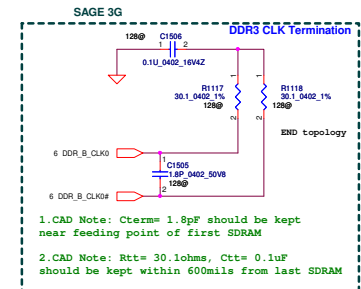
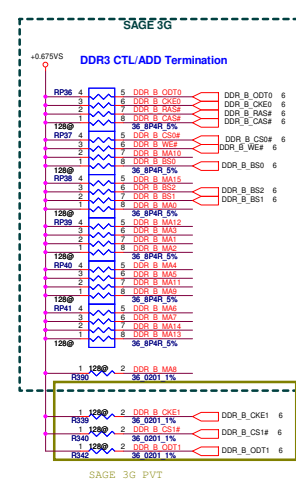
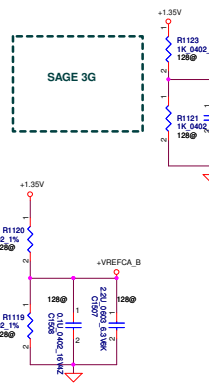
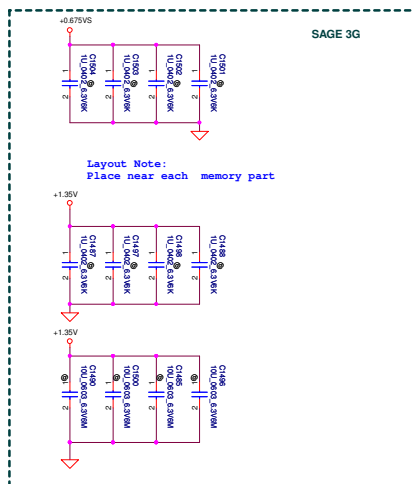
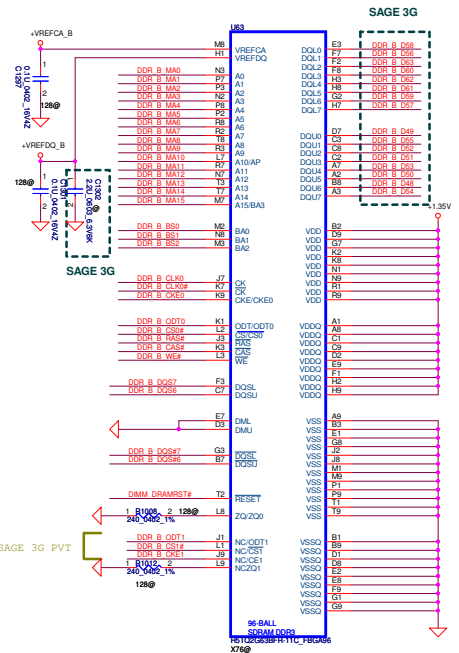
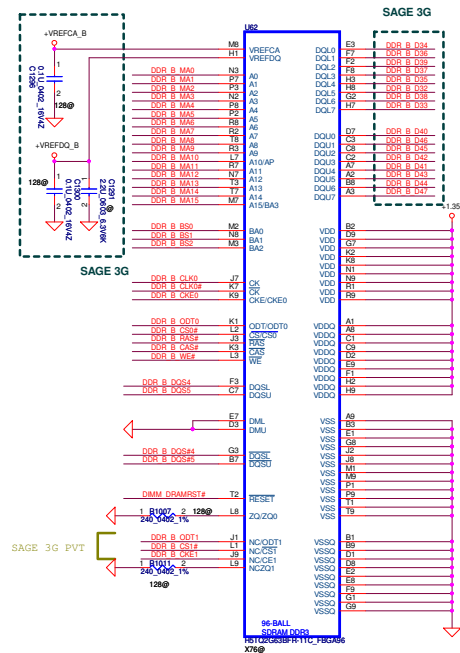
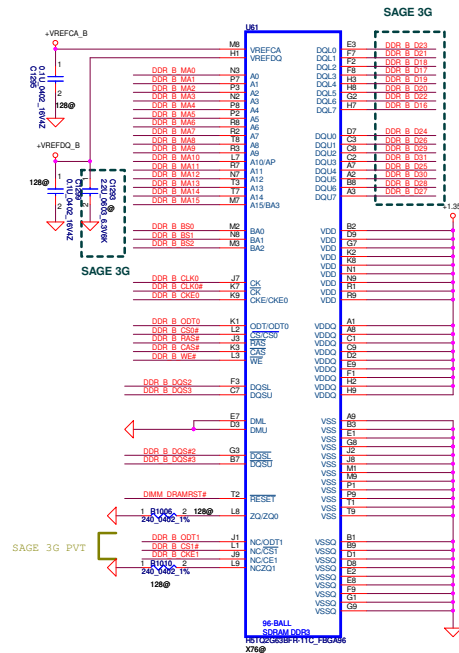
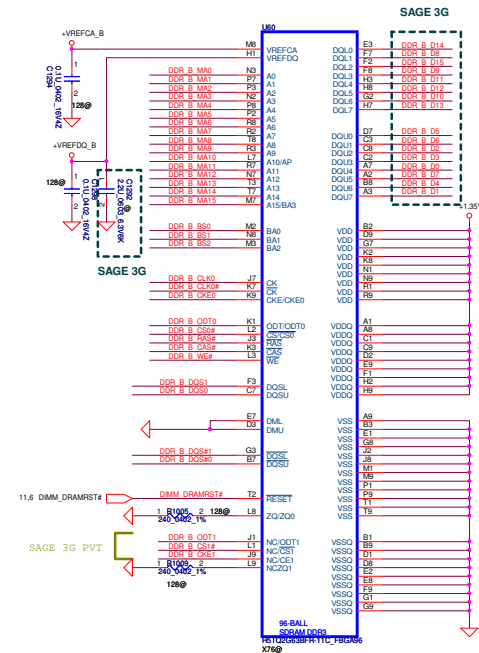
Channel A

- 6 DDR_A_MA0[0..15] DDR A MA0..15
- 6 DDR_A_DQS#0[0..7] DDR A DQS#0..7
- 6 DDR_A_DQS#0[0..7] DDR A DQS#0..7
- 6 DDR_A_DQS#0[0..7] DDR A DQS#0..7
- 6 DDR_A_DQ0[0..63] DDR A DQ0..63

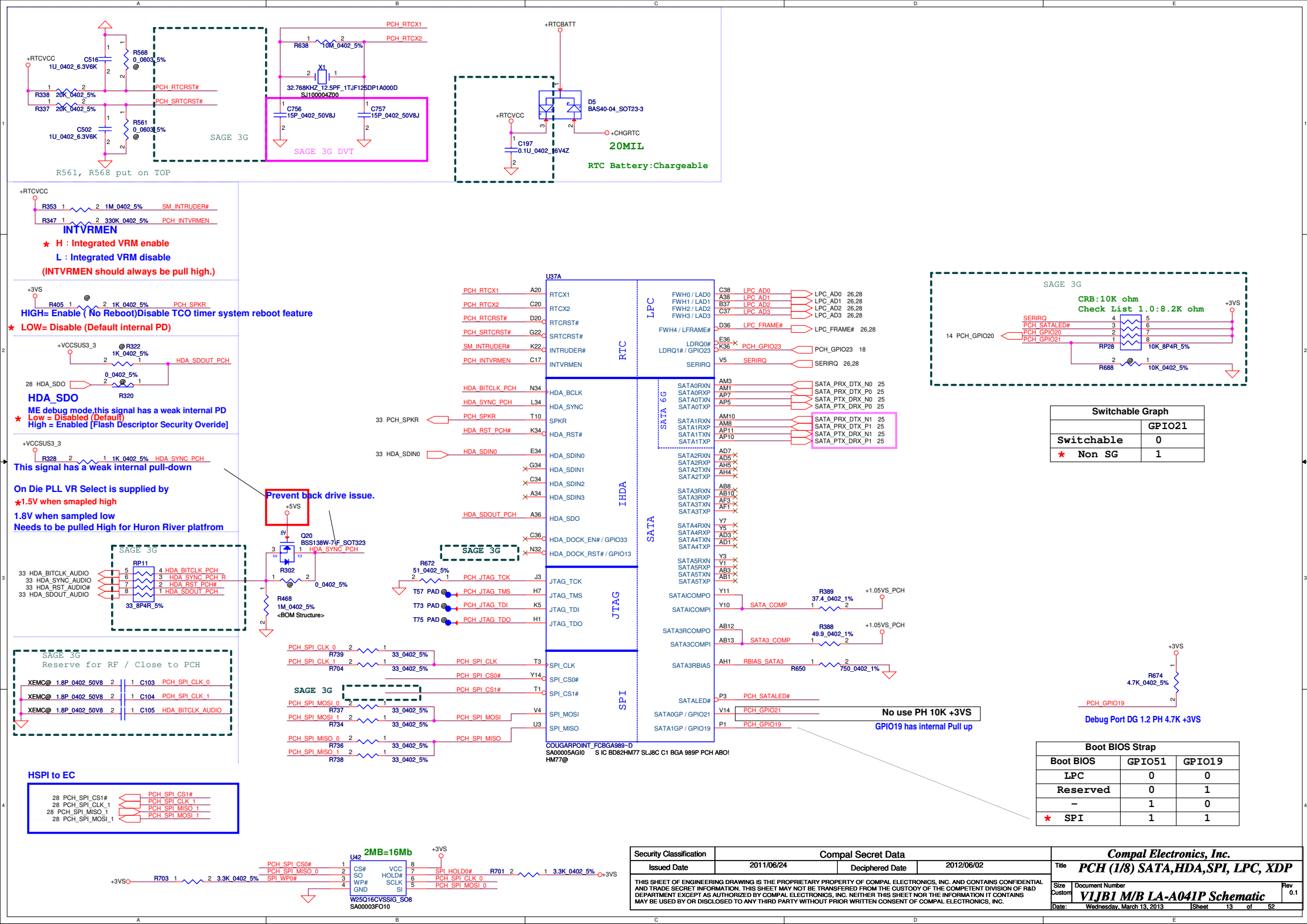


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/06/24		2012/07/12		DDRIII DIMMA	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
				V1J1B1 M/B LA-A041P Schematic	
Date:		Wednesday, March 13, 2013		Sheet	11 of 52

Channel B



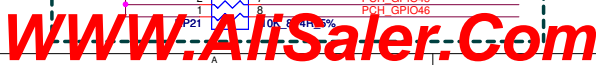
Security Classification	Compal Secret Data	Deciphered Date	2012/06/02
Issued Date	2011/06/24	Deciphered Date	2012/06/02
This SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. WITHIN THIS SHEET FOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			
File	Compal Electronics, Inc.		
Doc No.	DDRIII DIMMB		
Rev	1		
Drawn	VJ1B1 M/B LA-A041P Schematic		
Date	Wednesday, March 15, 2012		
Sheet	12 of 12		

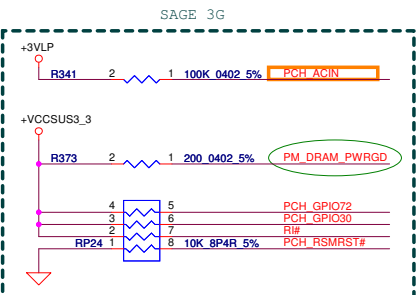


Switchable Graph	
Switchable	GPIO21
★ Non SG	1

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	PCH (1/8) SATA, HDA, SPI, LPC, XDP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size Custom	Document Number	V1JBI M/B LA-A041P Schematic		Rev	0.1
Date	Wednesday, March 13, 2013	Sheet	13	of	52

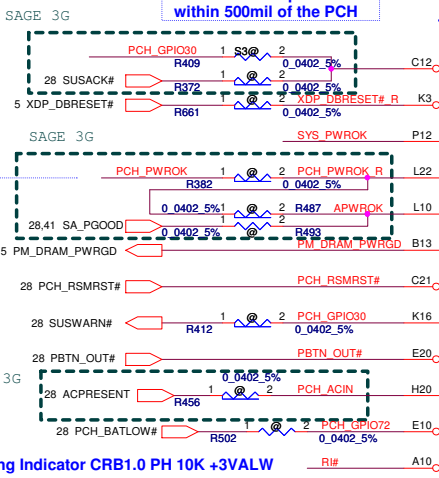
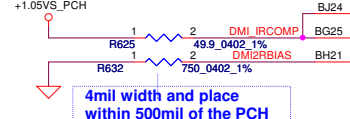
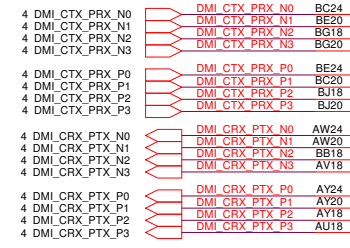
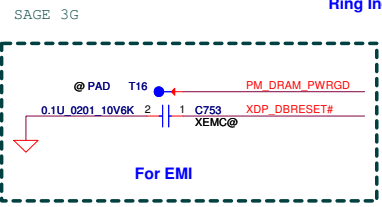




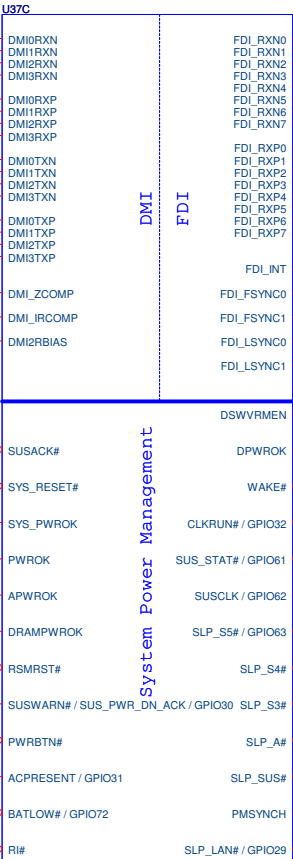
not support Deep S4,S5 mux with SUS_PWR_DN_ACK

not support AMT APWROK can mux with PWROK (check list1.0 P.40)

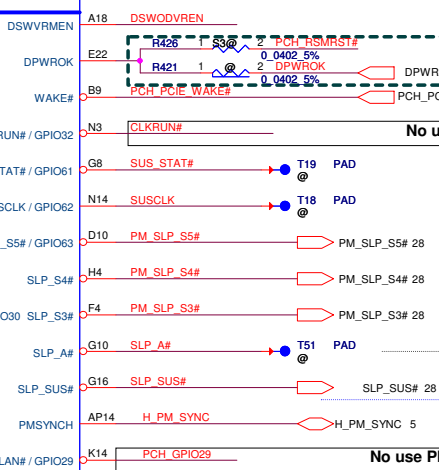
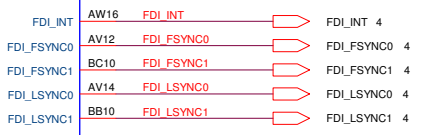
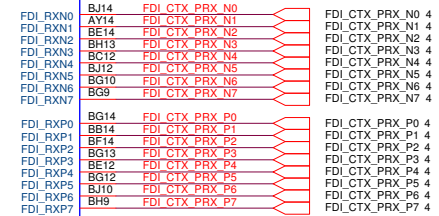
No use PH 10K +3VALW



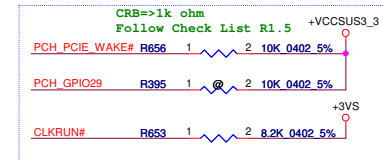
Ring Indicator CRB1.0 PH 10K +3VALW



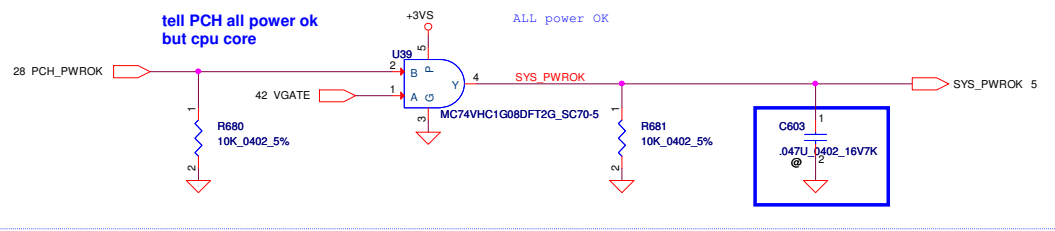
是否改為NC



not support Deep S4,S5 DPWROK mux with RSMRST# check list1.0 P.42



Can be left NC when IAMT is not support on the platform
not support Deep S4,S5 can NC PCH EDS1.2 P.74



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/24				PCH (3/8) DMI, FDI, PM			
Deciphered Date				2012/06/02				V1JBI M/B LA-A041P Schematic			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date				Wednesday, March 13, 2013			
				Sheet				15 of 52			
								Rev 0.1			

UMA Panel Backlight ON/OFF

28 ENBKL ENBKL R612 2 @ 1 0_0402_5% IGPU BKLT_EN

PD 100K
at EC side

Delete LVDS function

LVDS disable:
DATA/Clock/Control can NC
VCC_TX_LVDS,VCCA_LVDS connected to GND

CRT disable:
DATA/Clock/Control can NC
DAC_IREF still need PD
VCCADAC connected to +3VS

For CRT diable
=>Change 1K 0.5% to 5%

R307
1K_0402_5%

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

101

102

103

104

105

106

107

108

109

110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

125

126

127

128

129

130

131

132

133

134

135

136

137

138

139

140

141

142

143

144

145

146

147

148

149

150

151

152

153

154

155

156

157

158

159

160

161

162

163

164

165

166

167

168

169

170

171

172

173

174

175

176

177

178

179

180

181

182

183

184

185

186

187

188

189

190

191

192

193

194

195

196

197

198

199

200

201

202

203

204

205

206

207

208

209

210

211

212

213

214

215

216

217

218

219

220

221

222

223

224

225

226

227

228

229

230

231

232

233

234

235

236

237

238

239

240

241

242

243

244

245

246

247

248

249

250

251

252

253

254

255

256

257

258

259

260

261

262

263

264

265

266

267

268

269

270

271

272

273

274

275

276

277

278

279

280

281

282

283

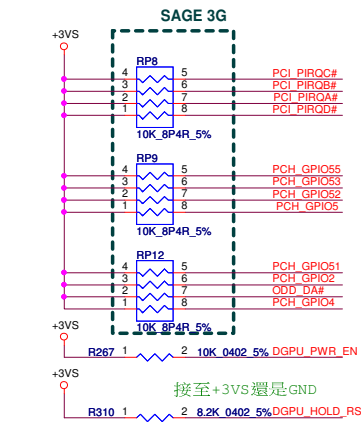
284

285

286

287

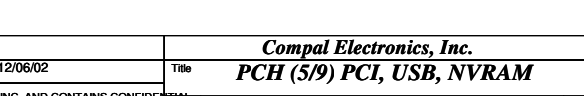
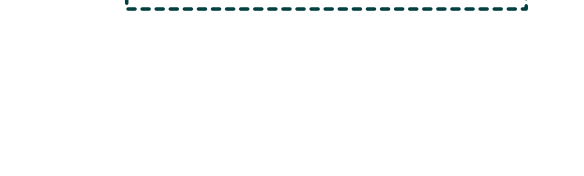
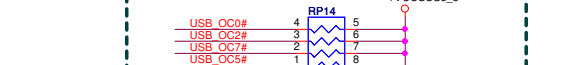
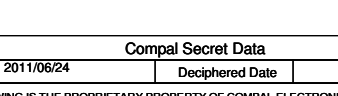
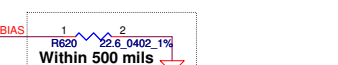
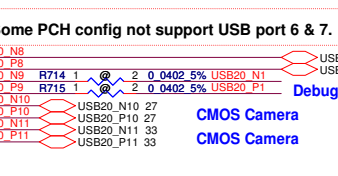
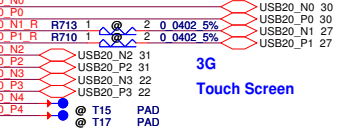
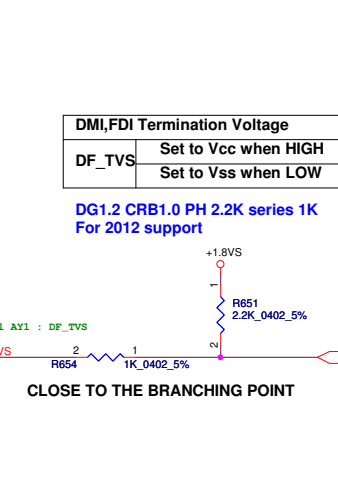
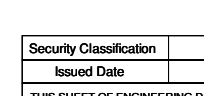
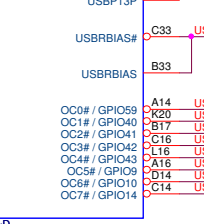
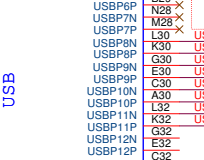
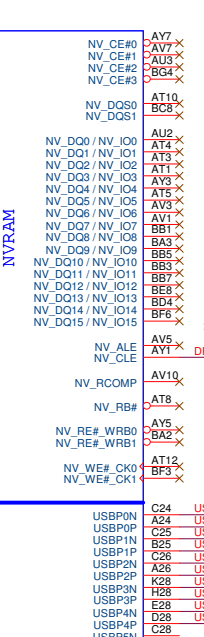
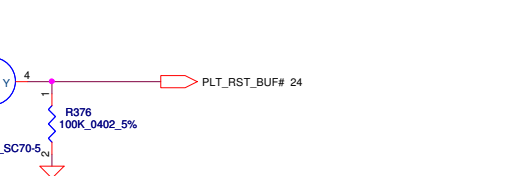
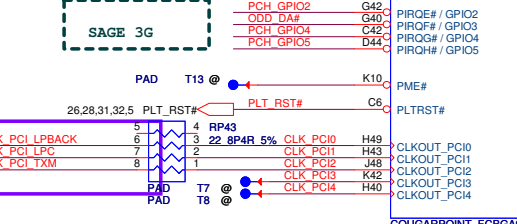
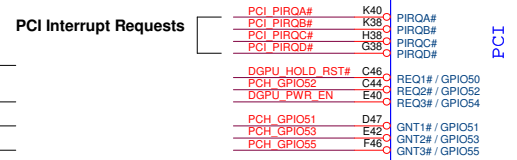
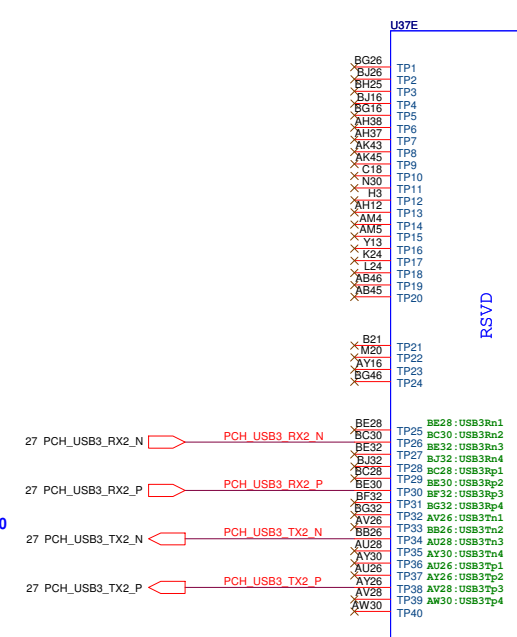
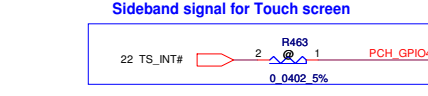
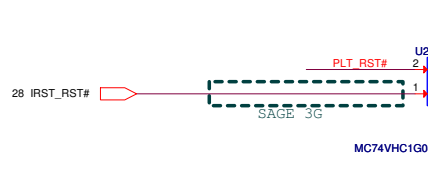
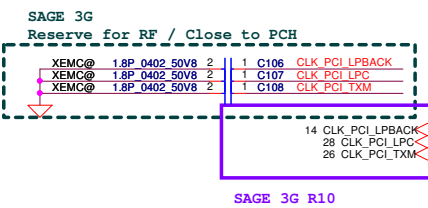
288



Boot BIOS Strap			
GNT1#/ GPIO51	GPIO19 GPIO51		Boot BIOS
	Bit11	Bit10	Destination
Internal PH	0	1	Reserved
	1	0	PCI
PH	1	1	SPI
	0	0	LPC

只剩GPIO的功能沒有strap function
不做GPIO要PH +3VS,如做GPIO PH +3VS

只剩GPIO的功能沒有strap function
無須PH(Internal PH),如做GPIO PH +3VS

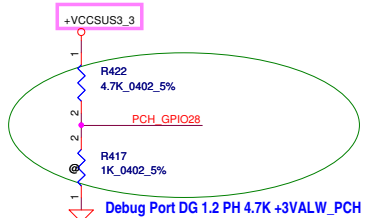


HDA_SYNC PH(PLL =+1.5VS)

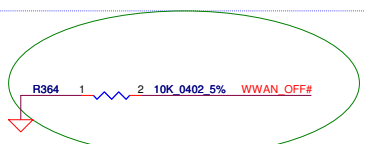
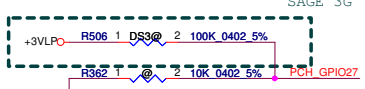
GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up
 * H : On-Die PLL voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal RTC alarm,Power BTN,GPIO27 PCH_GPIO27 (Have internal Pull-High)

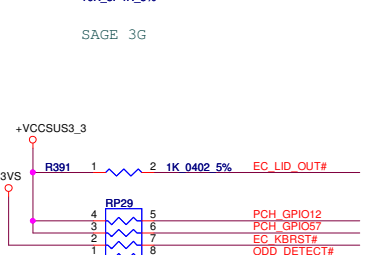
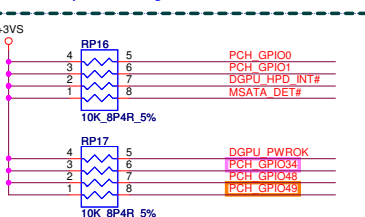


SATA2GP/GPIO36,SATA3GP/GPIO37

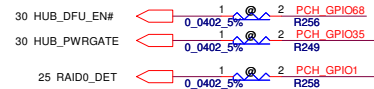
1.Used as for Mechanical Presence detect -
 use a weak external pull-up (150K-200k Ohms) to Vcc3_3
 or use 10K external pull-up that is enabled only
 after PLTRST# de-assertion.

2.Used as GP Input (Pin HW default) -
 Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA*GP -
 Use 8.2K-10K pull-down to ground.



GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration
 register bits are not cleared by
 CF9h reset event.
 CRB1.0 PH10K to +3VALW



No use PH 10K +3VS	PCH_GPIO0	T7
No use PH 10K +3VS	PCH_GPIO1	A42
No use PH 10K +3VS	DGPU_HPDI_INT#	H36

No use PH +3VALW	PCH_GPIO2	C4
No use PH +3VALW	EC LID SW OUT	G2
No use PH +3VS	MSATA_DET#	U2

No use PH 10K +3VS	PCH_GPIO22	T5
CRB1.0 PH 10K +3VALW	PCH_GPIO24	E8
No use PD 10K to GND	EC_DS3_WAKE#	E16
No use PH 10K +3VALW	PCH_GPIO27	P8
No use PH 10K +3VS	PCH_GPIO28	K1
No use PH 10K +3VS	PCH_GPIO34	K4
No use PH 10K +3VS	PCH_GPIO35	K4
No use PH 10K +3VS	PCH_GPIO36	V8
No use PH 10K +3VS	PCH_GPIO37	M5
No use PH 10K +3VS	PCH_GPIO38	N2
No use PH 10K +3VS	PCH_GPIO39	M3
No use PH 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	PCH_GPIO49	V3
No use PH +3VALW	PCH_GPIO57	D6

GPIO38 OPTIMUS_EN#	
Muxless	0
nonMuxless	1

Define Q5LJ1 (DDR3) or V1JV1 (DDR3L)

GPIO24 PCH_GPIO24	
DDR3L(V1JV1)	0
DDR3	1

GPIO36/GPIO37 is Strap functionality
 that requires internal pull down to be sampled at rising PWROK.
 When uses as SATA2GP/SATA3GP for mechanical presence detect
 -use a external pull up 150K-200K ohm to Vcc3_3
 When used as GP input
 -ensure GPI is not driven high during strap sampling window
 When Unused as GPIO or SATA*GP
 -use 8.2K-10K pull-down
 check list page 47

U37F

BMBUSY# / GPIO0	T7
TACH1 / GPIO1	A42
TACH2 / GPIO6	E38
TACH3 / GPIO7	C10
GPIO8	C4
LAN_PHY_PWR_CTRL / GPIO12	G2
GPIO15	U2
SATA4GP / GPIO16	D40
TACH0 / GPIO17	E8
SCLOCK / GPIO22	E16
GPIO24 / MEM_LED	P8
GPIO27	K1
GPIO28	K4
STP_PC# / GPIO34	V8
GPIO35	M5
SATA2GP / GPIO36	N2
SATA3GP / GPIO37	M3
SLOAD / GPIO38	V13
SDATAOUT0 / GPIO39	V3
SDATAOUT1 / GPIO48	D6
SATA5GP / GPIO49	
GPIO57	

VSS_NCTF_1	A4
VSS_NCTF_2	A44
VSS_NCTF_3	A45
VSS_NCTF_4	A5
VSS_NCTF_5	A6
VSS_NCTF_6	B3
VSS_NCTF_7	B47
VSS_NCTF_8	BD1
VSS_NCTF_9	BD49
VSS_NCTF_10	BE1
VSS_NCTF_11	BE49
VSS_NCTF_12	BF1
VSS_NCTF_13	BF49
VSS_NCTF_14	

COUGARPOINT_FCBGA888-D
 SA00005AGIO S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABOI
 HM77@

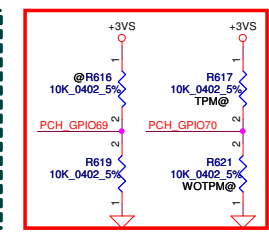
GPIO

NCTF

TACH4 / GPIO68	C40
TACH5 / GPIO69	B41
TACH6 / GPIO70	C41
TACH7 / GPIO71	A40

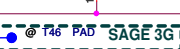
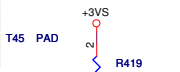
A20GATE	P4
PECI	AU16
RCIN#	P5
PROCPWRGD	AY11
THRMTRIP#	AY10
INIT3_3V#	T14
NC_1	AH8
NC_2	AK11
NC_3	AH10
NC_4	AK10
NC_5	P37

VSS_NCTF_15	BG2
VSS_NCTF_16	BG48
VSS_NCTF_17	BH3
VSS_NCTF_18	BH47
VSS_NCTF_19	BJ4
VSS_NCTF_20	BJ44
VSS_NCTF_21	BJ45
VSS_NCTF_22	BJ46
VSS_NCTF_23	BJ5
VSS_NCTF_24	BJ6
VSS_NCTF_25	C2
VSS_NCTF_26	C48
VSS_NCTF_27	D1
VSS_NCTF_28	D49
VSS_NCTF_29	E1
VSS_NCTF_30	E49
VSS_NCTF_31	F1
VSS_NCTF_32	F49



SW base on TPM table to detect HW TPM status

TPM Status	GPIO69	GPIO70
HW, SW without support TPM	0	0
Infinion TPM SLB9655	0	1
X	1	0
X	1	1



INIT3_3V Check list1.0 P.59
 This signal has weak internal
 PU, can't pull low,leave NC

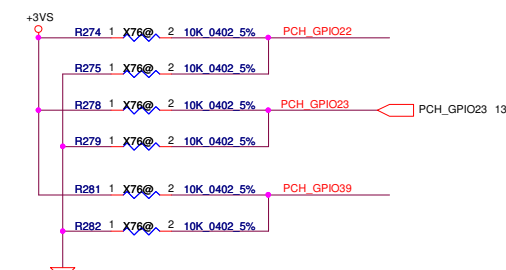
TS_VSS1~4
 PD to GND



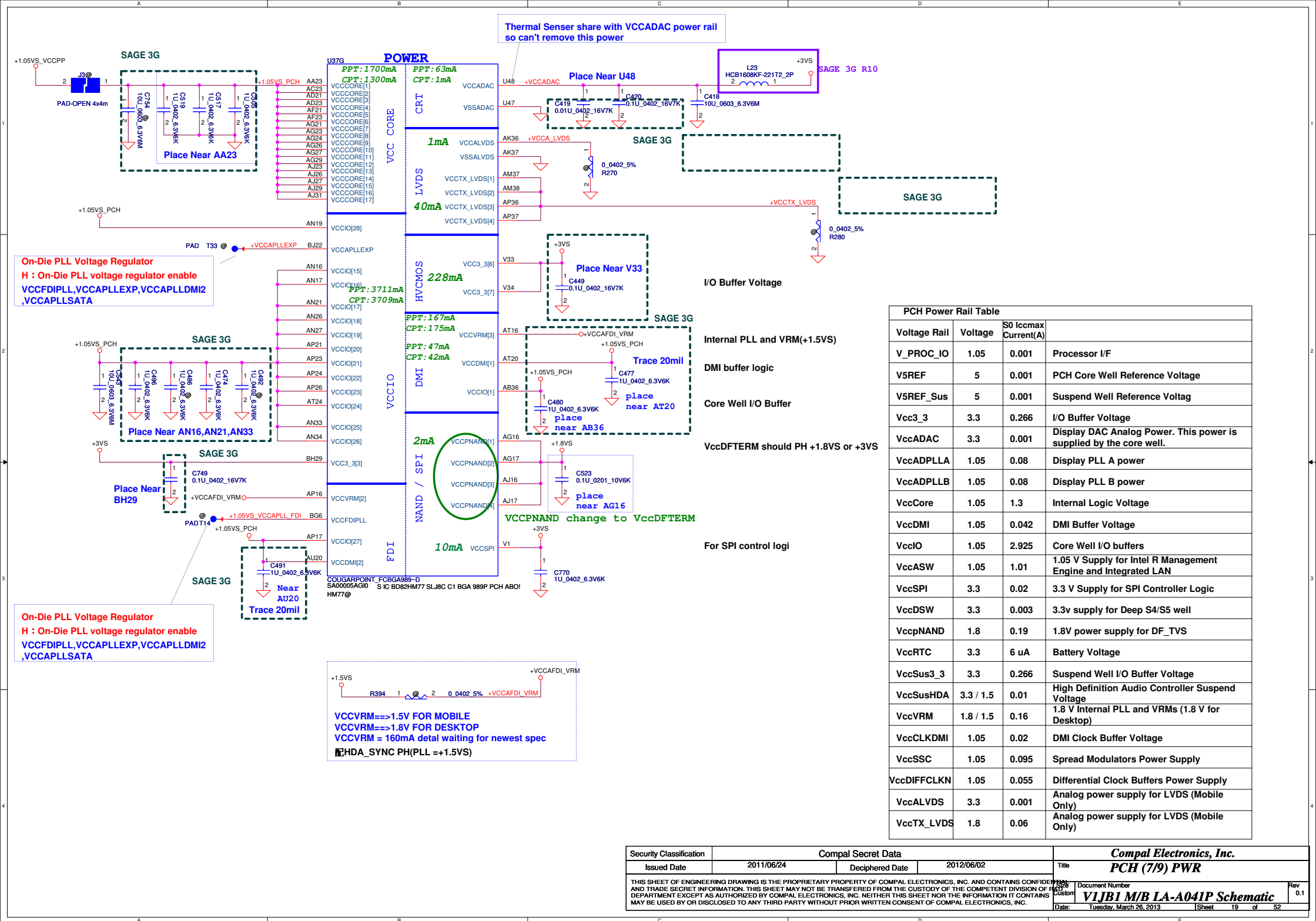
SA000059110 / ELPIDA DDR3L-1333
 SA00005FV10 / HYNIX DDR3L-1333
 SA00005HT80 / ELPIDA DDR3L-1600

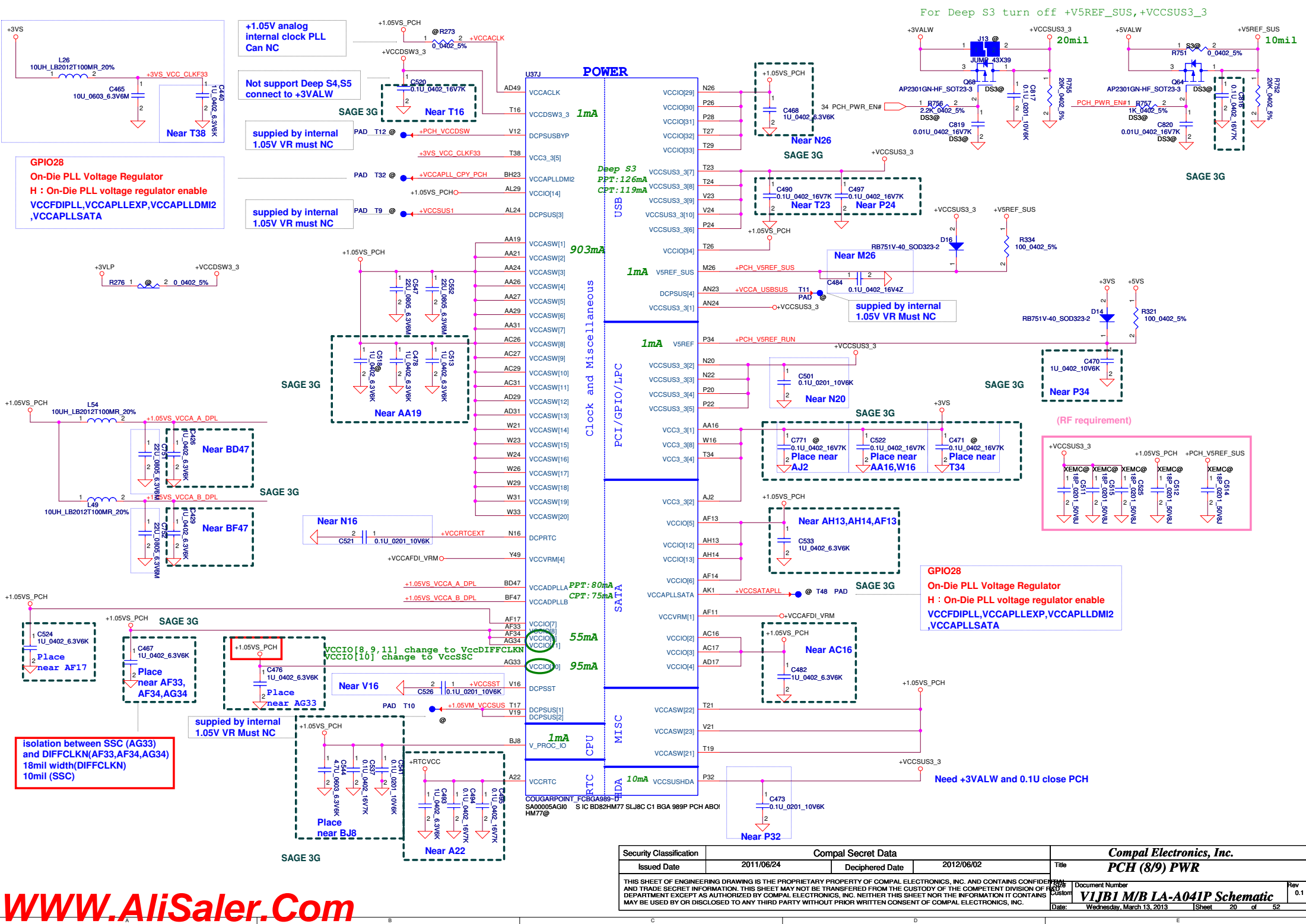
DDR3L-1333
 DDR3L-1333
 DDR3L-1333
 DDR3L-1333
 DDR3L-1600
 DDR3L-1600
 DDR3L-1600

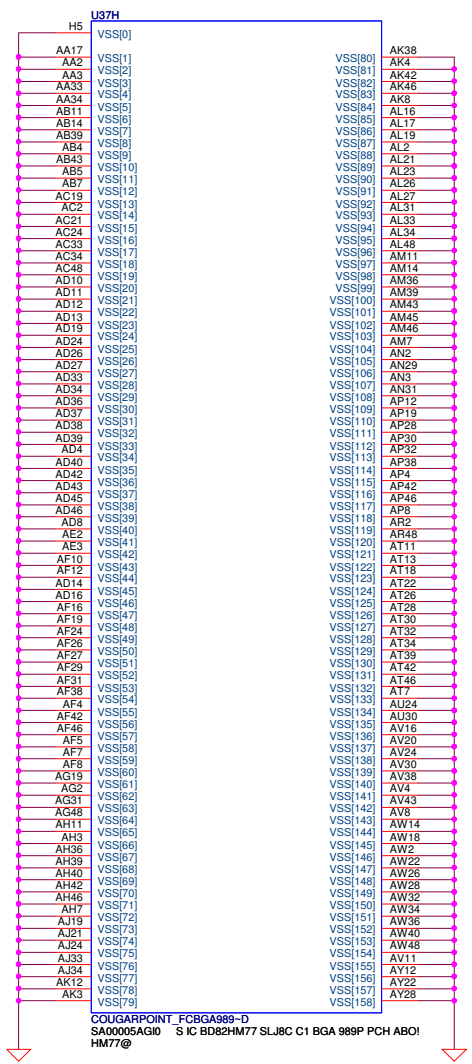
	GPIO39	GPIO23	GPIO22
Elpida Mono 512MB*4 (Ch A)	0	0	0
Hynix Mono 512MB*4 (Ch A)	0	0	1
Elpida Mono 512MB*8 (Ch A,B)	0	1	0
Hynix Mono 512MB*8 (Ch A,B)	0	1	1
Elpida Mono 512MB*4 (Ch A)	1	0	0
DDR3L-1600	1	0	1
DDR3L-1600	1	1	0
DDR3L-1600	1	1	1



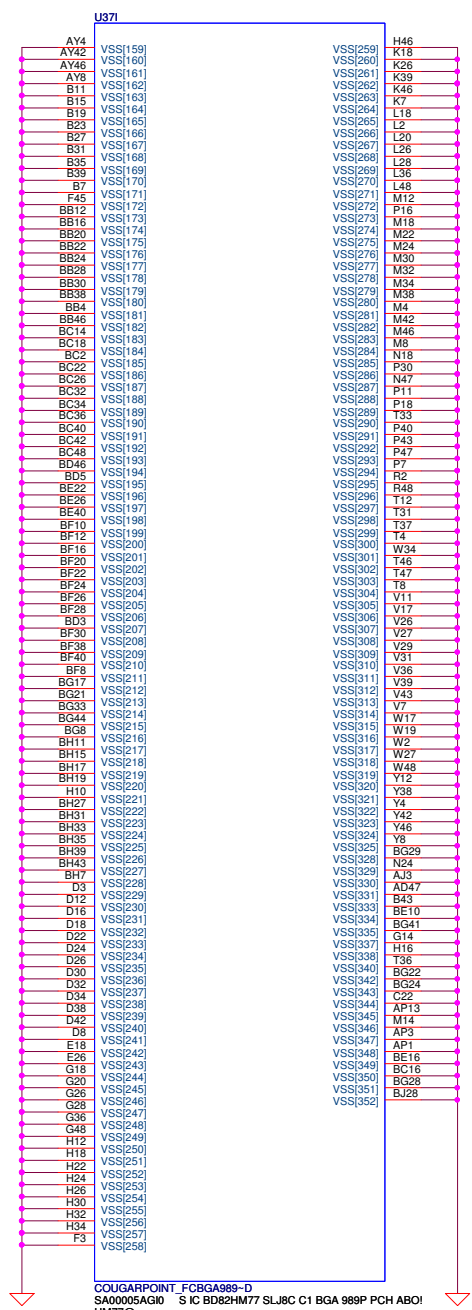
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/24	Deciphered Date	2012/06/02	PCH (6/9) GPIO, CPU, MISC		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS SHALL BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	V1JB1 M/B LA-A041P Schematic	Rev 0.1
				Date:	Wednesday, March 13, 2013	Sheet 18 of 52







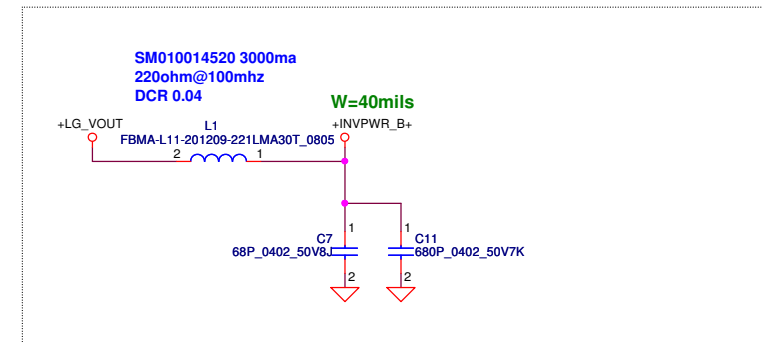
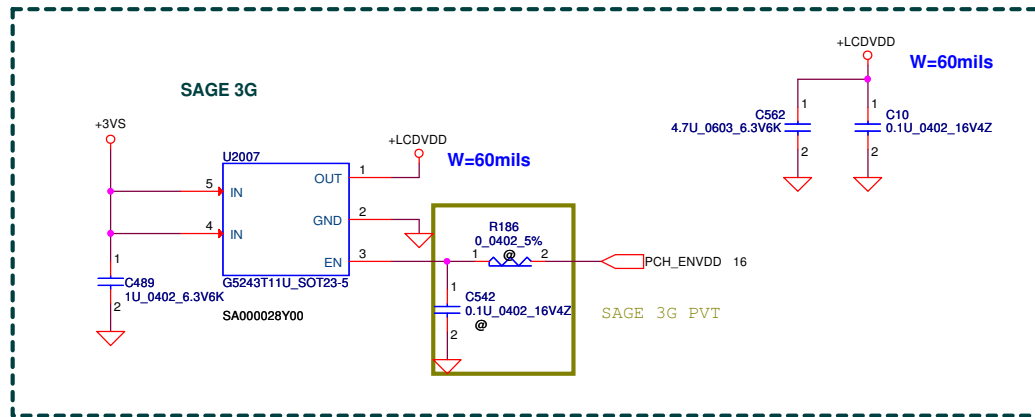
COUGARPOINT_FCBGA989-D
SA00005AG10 S IC B082HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@



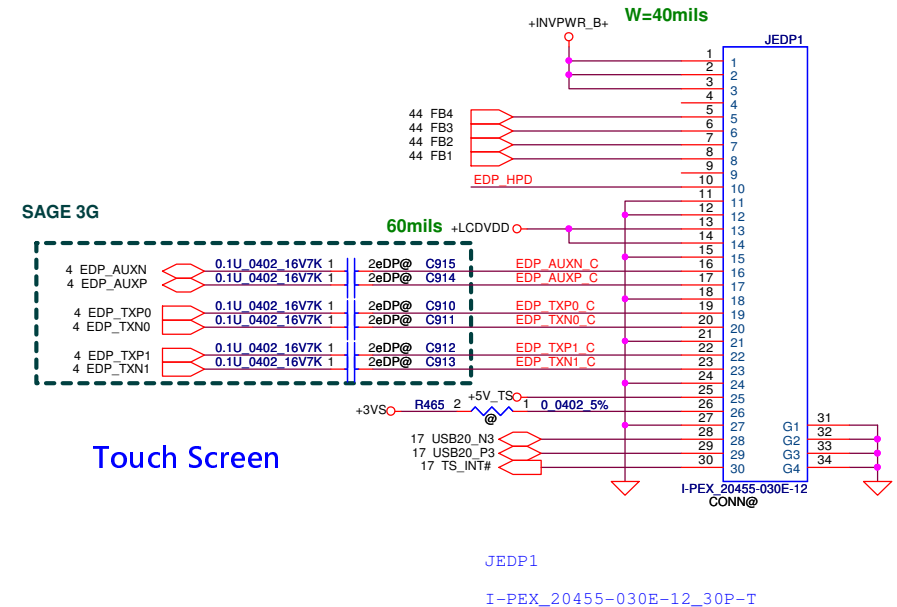
COUGARPOINT_FCBGA989-D
SA00005AG10 S IC B082HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@

Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/06/24		Deciphered Date		2012/06/02		Title	
								PCH (9/9) VSS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Revision		Rev	
						0.1		0.1	
						VIJBI M/B LA-A041P Schematic			
						Date: Wednesday, March 13, 2013		Sheet 21 of 52	

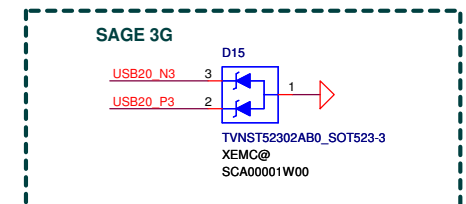
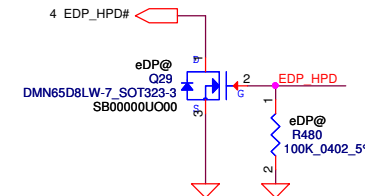
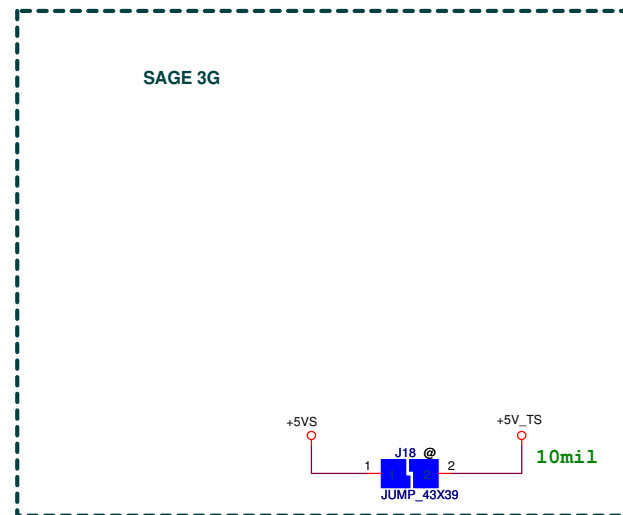
Panel POWER CIRCUIT



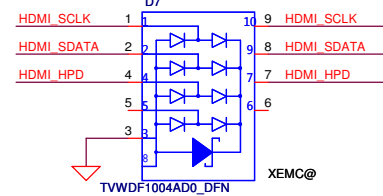
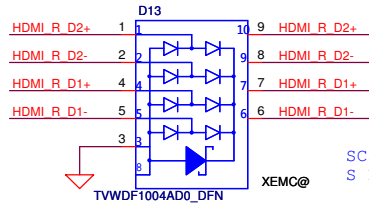
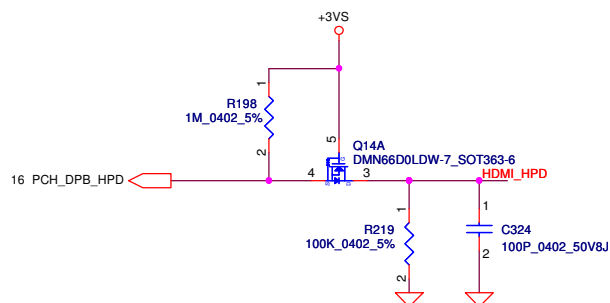
eDP PANEL Conn.



Touch Screen

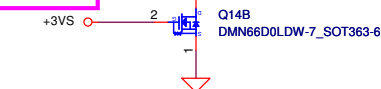
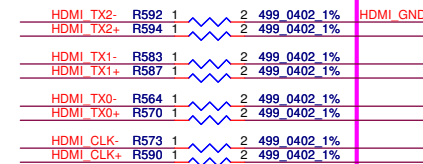
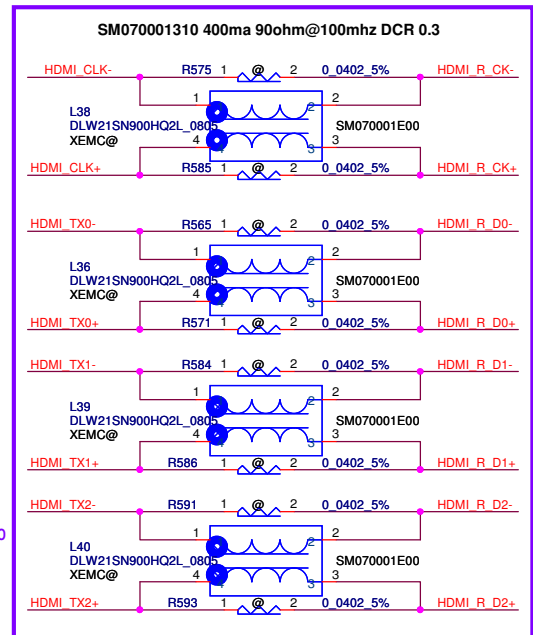


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	LVDS Connector
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
				Customer	V1JB1 M/B LA-A041P Schematic
				Date	Wednesday, March 13, 2013
				Sheet	22 of 52

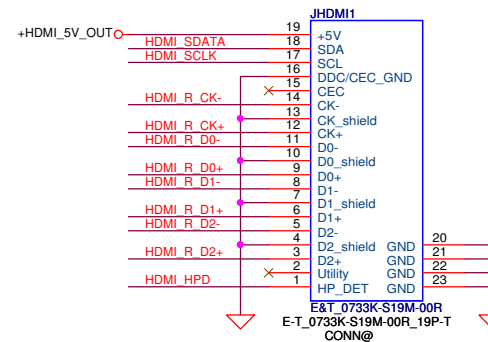


SC300002800
S DIO(BR) TVWDF1004AD0 DFN ESD

SAGE 3G R10

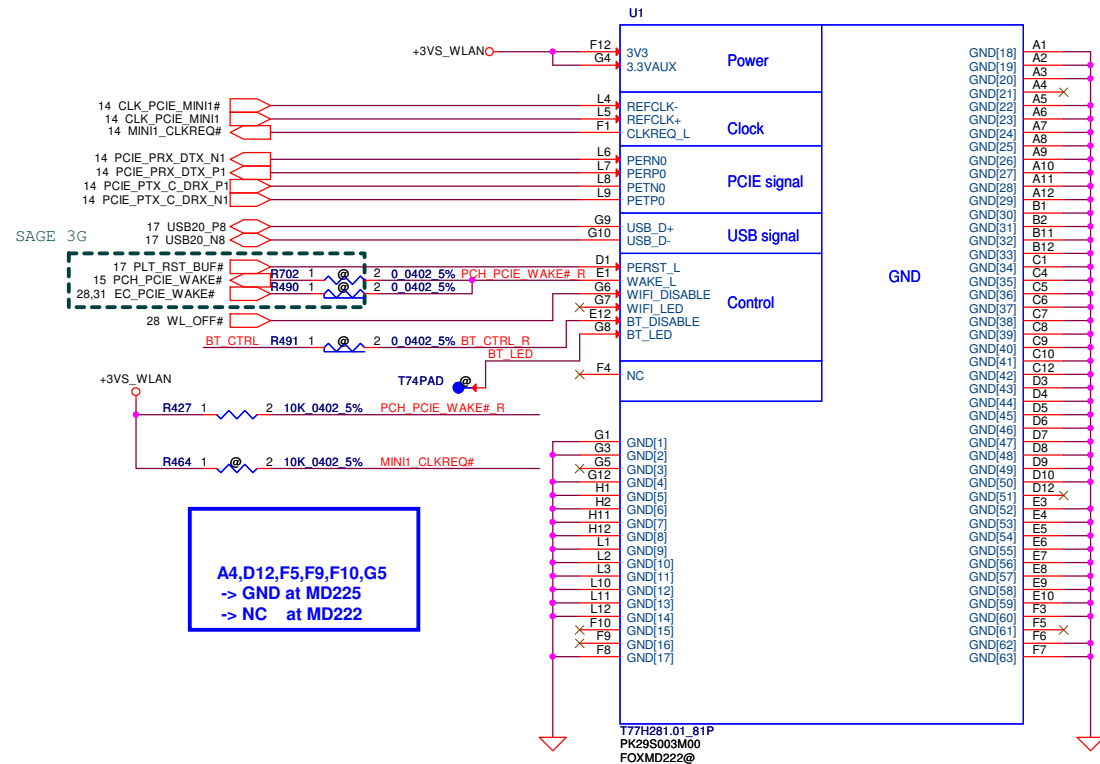
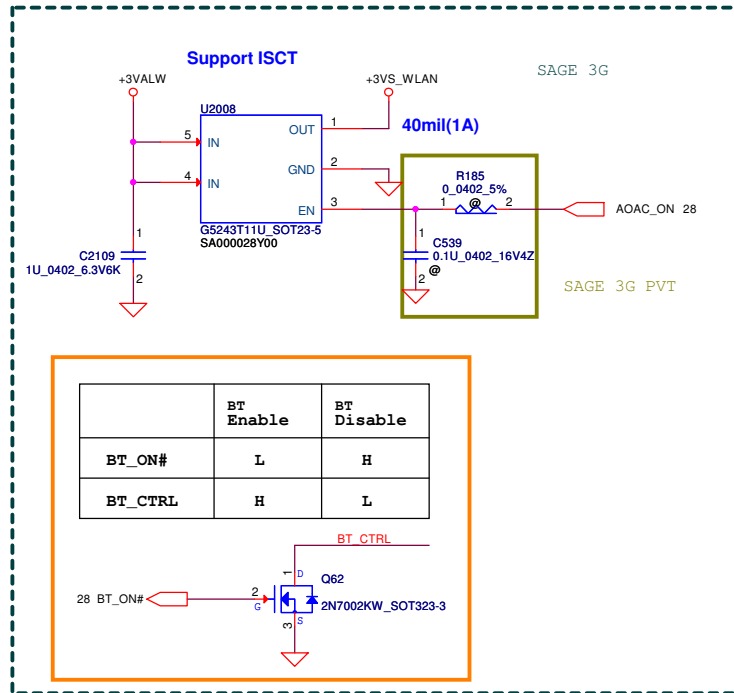
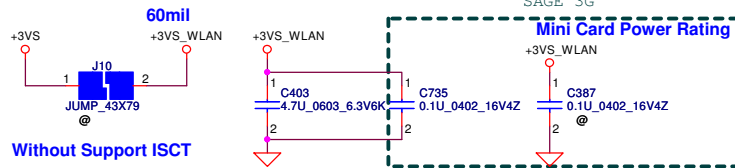


Micro HDMI connector
PCB Footprint : E-T_0733K-S19M-00R_19P-T-S



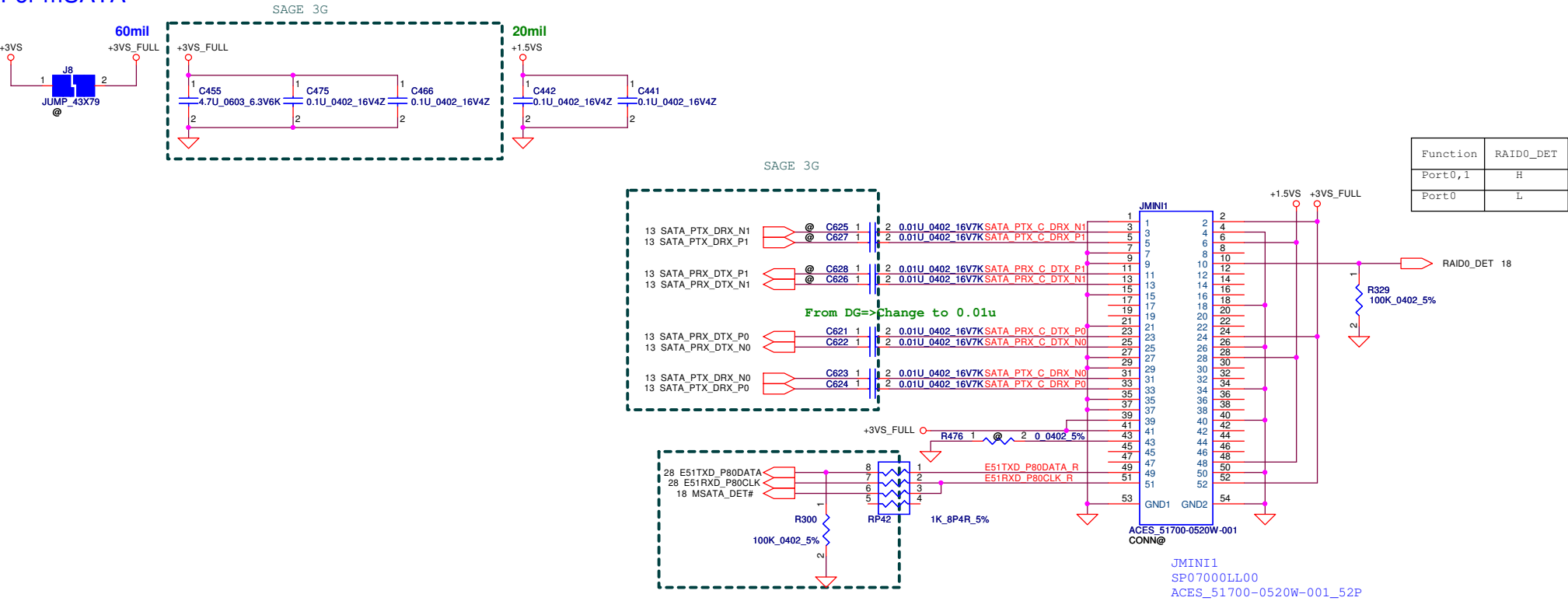
Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	HDMI Connector		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev	
				Custom	V1JB1 M/B LA-A041P Schematic	0.1	
				Date:	Tuesday, March 26, 2013	Sheet	23 of 52

For Wireless LAN

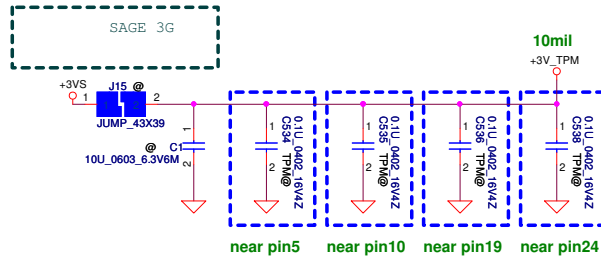


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				On Board WLAN	
Size		Document Number		Rev	
Custom		V1JB1 M/B LA-A041P Schematic		0.1	
Date:		Wednesday, March 13, 2013		Sheet 24 of 52	

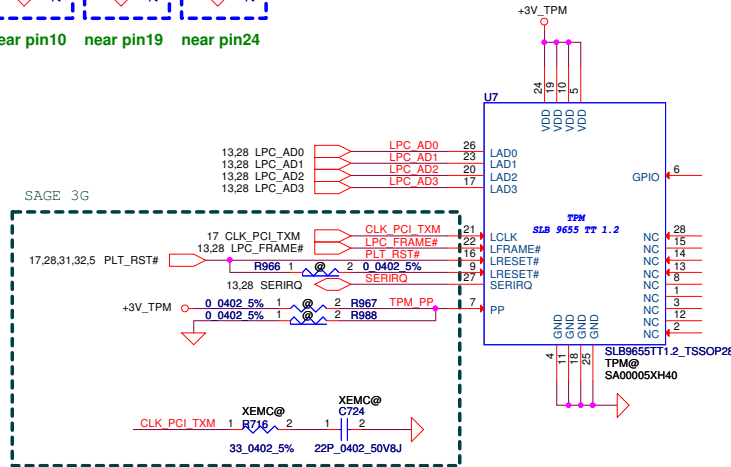
For mSATA



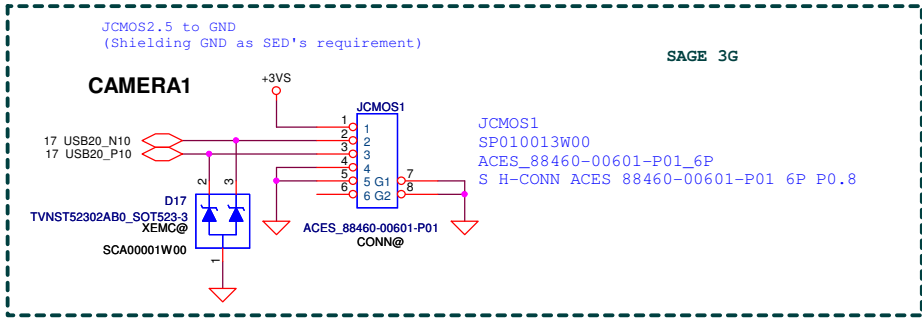
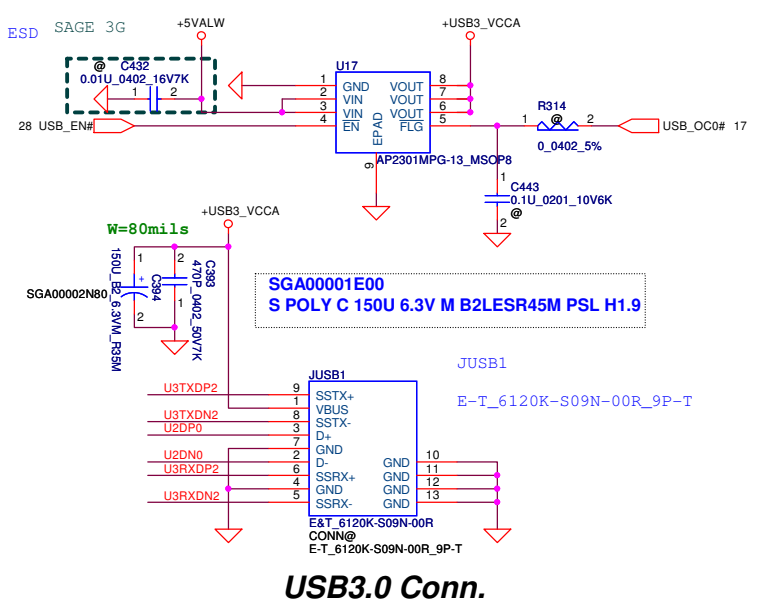
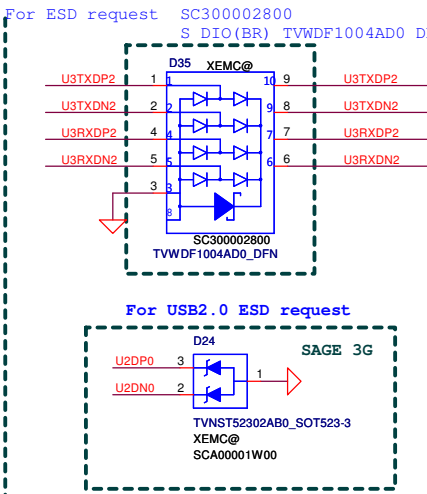
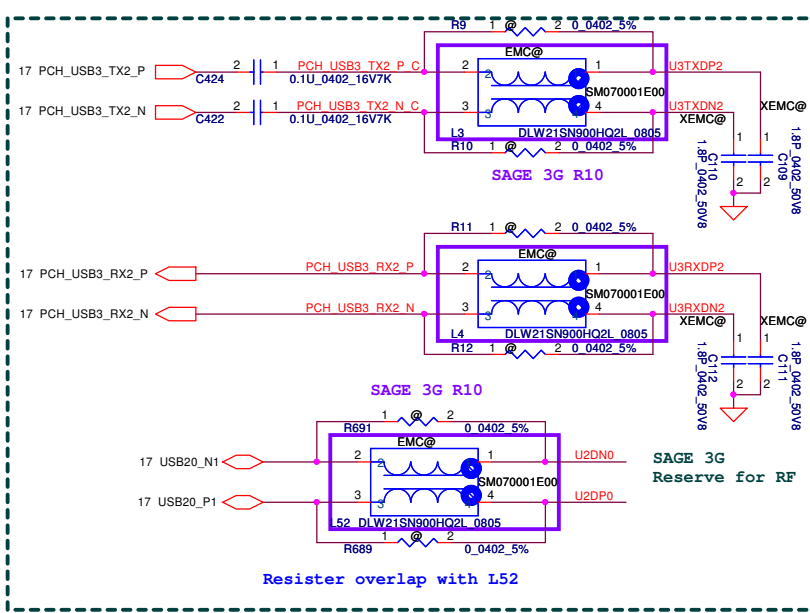
TPM



TPM - Infineon
SA00005XH40
S IC SLB9655TT1.2 FW4.31 TSSOP 28P TPM



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/11/1	Deciphered Date	2011/11/1	Title	TPM Infineon-SLB9655
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	V1JB1 M/B LA-A041P Schematic
				Date	Wednesday, March 13, 2013
				Sheet	26 of 52
				Rev	0.1

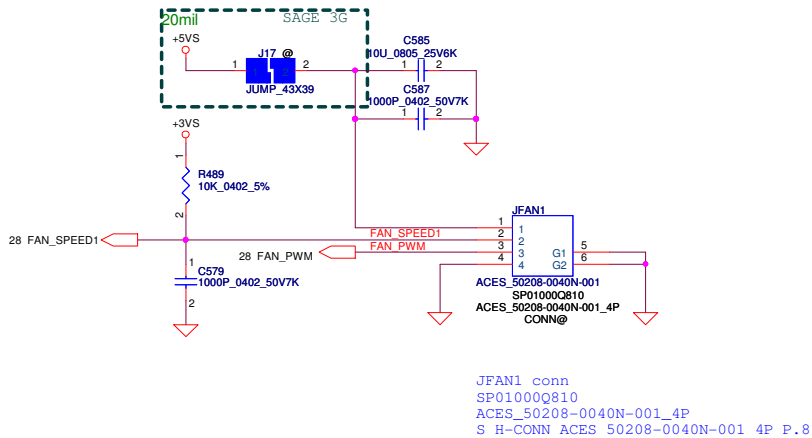


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/06/13	USB3.0	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				V1JB1 M/B LA-A041P Schematic	
				Date: Tuesday, March 26, 2013	Rev 0.1
				Sheet 27 of 52	



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	EC ITE-IT8518	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev	
				Customer	0.1	
Date:	Wednesday, March 13, 2013			Sheet	28 of 52	

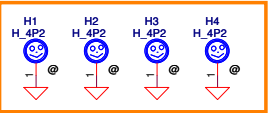
FAN Conn



定位孔



Thermal module



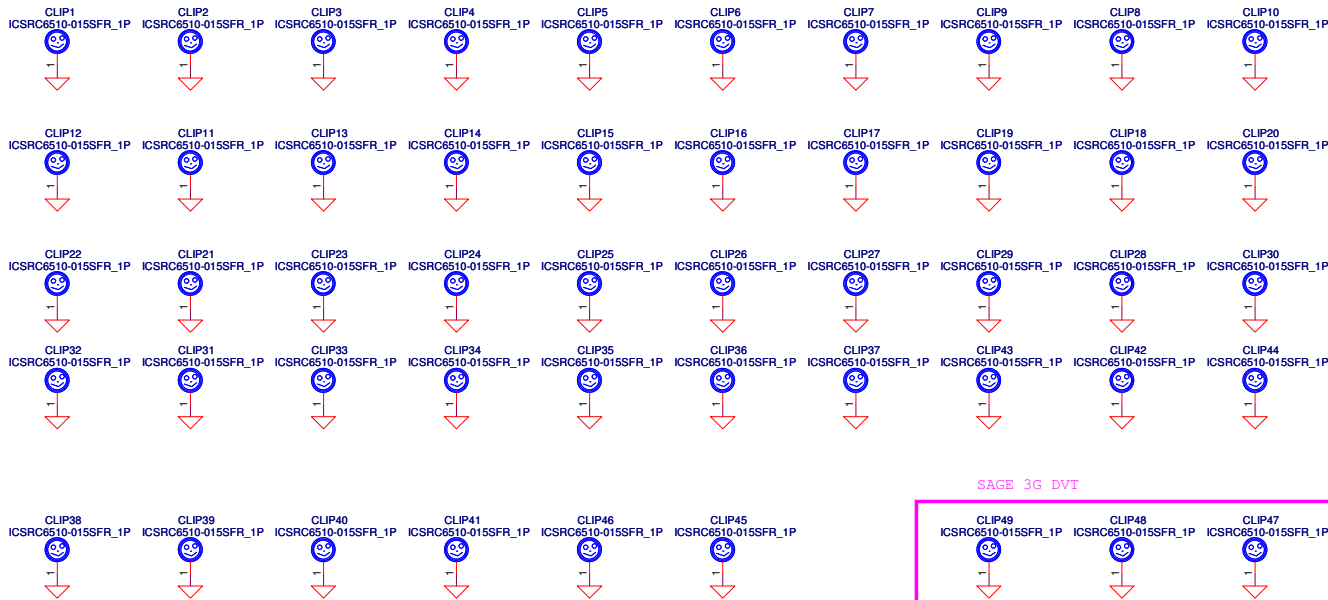
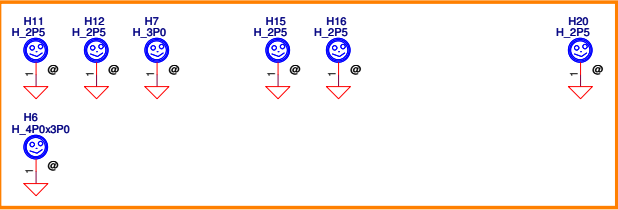
mSATA Stand-Off



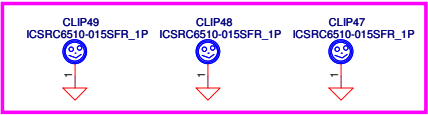
3G Stand-Off



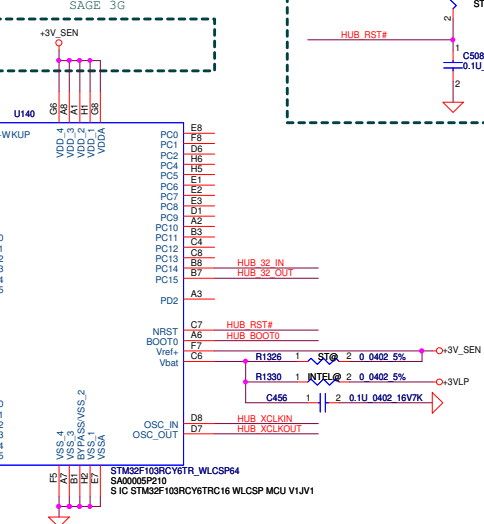
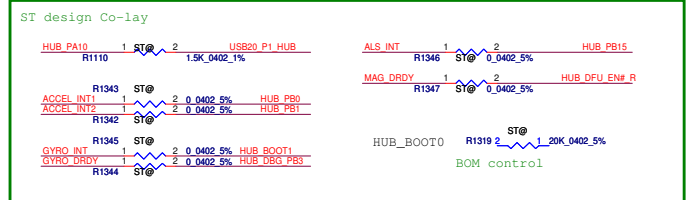
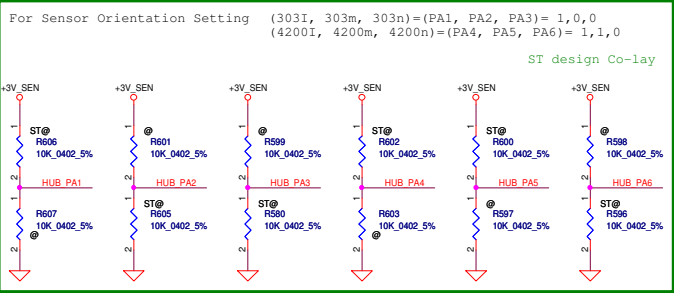
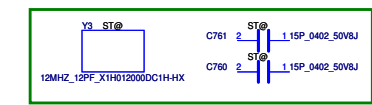
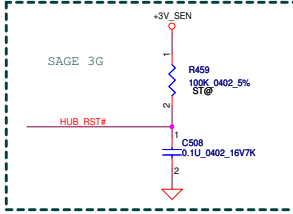
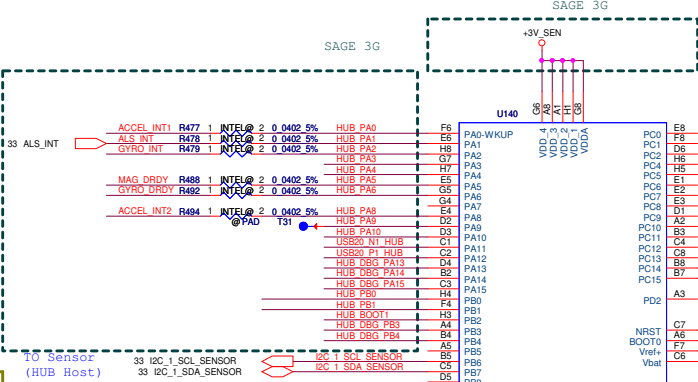
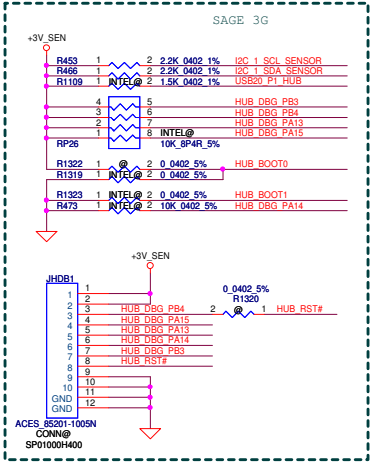
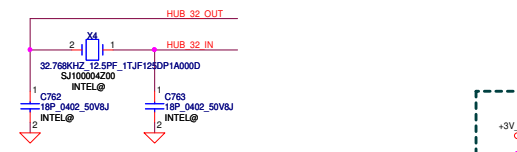
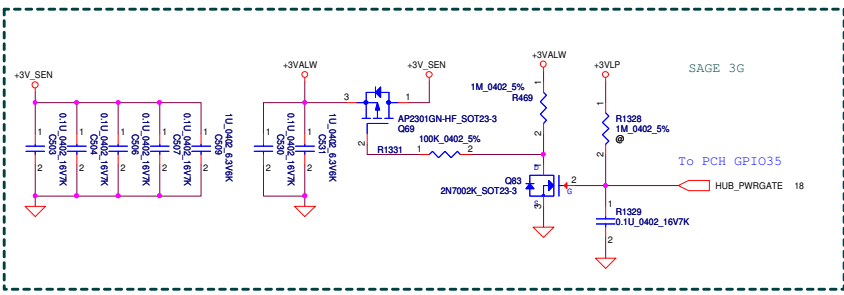
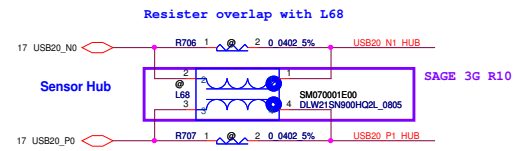
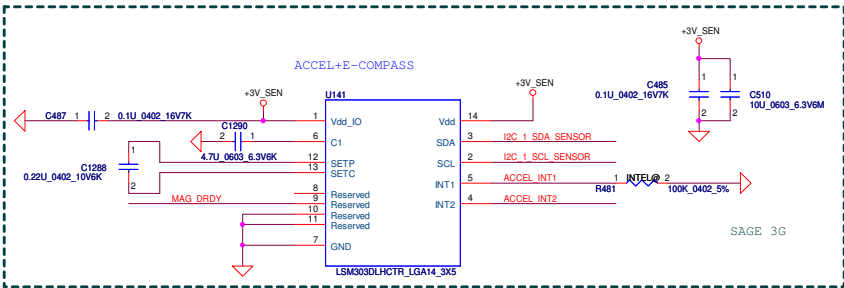
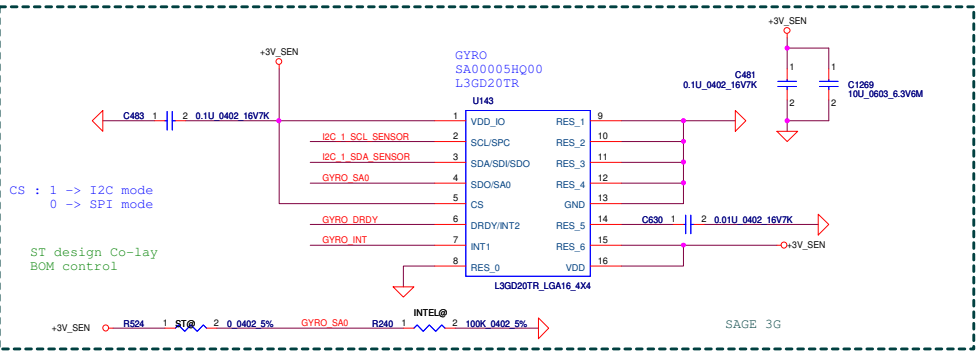
螺孔



SAGE 3G DVT

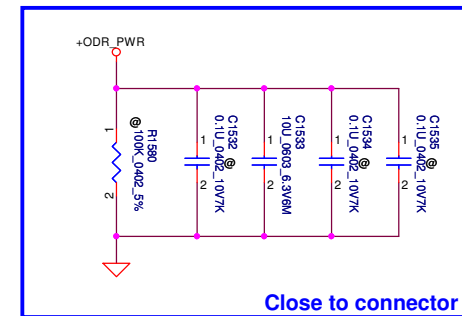
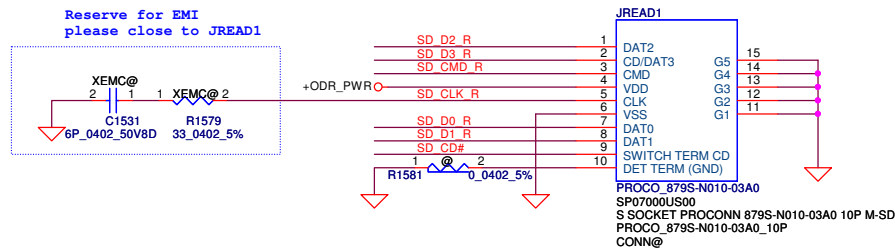
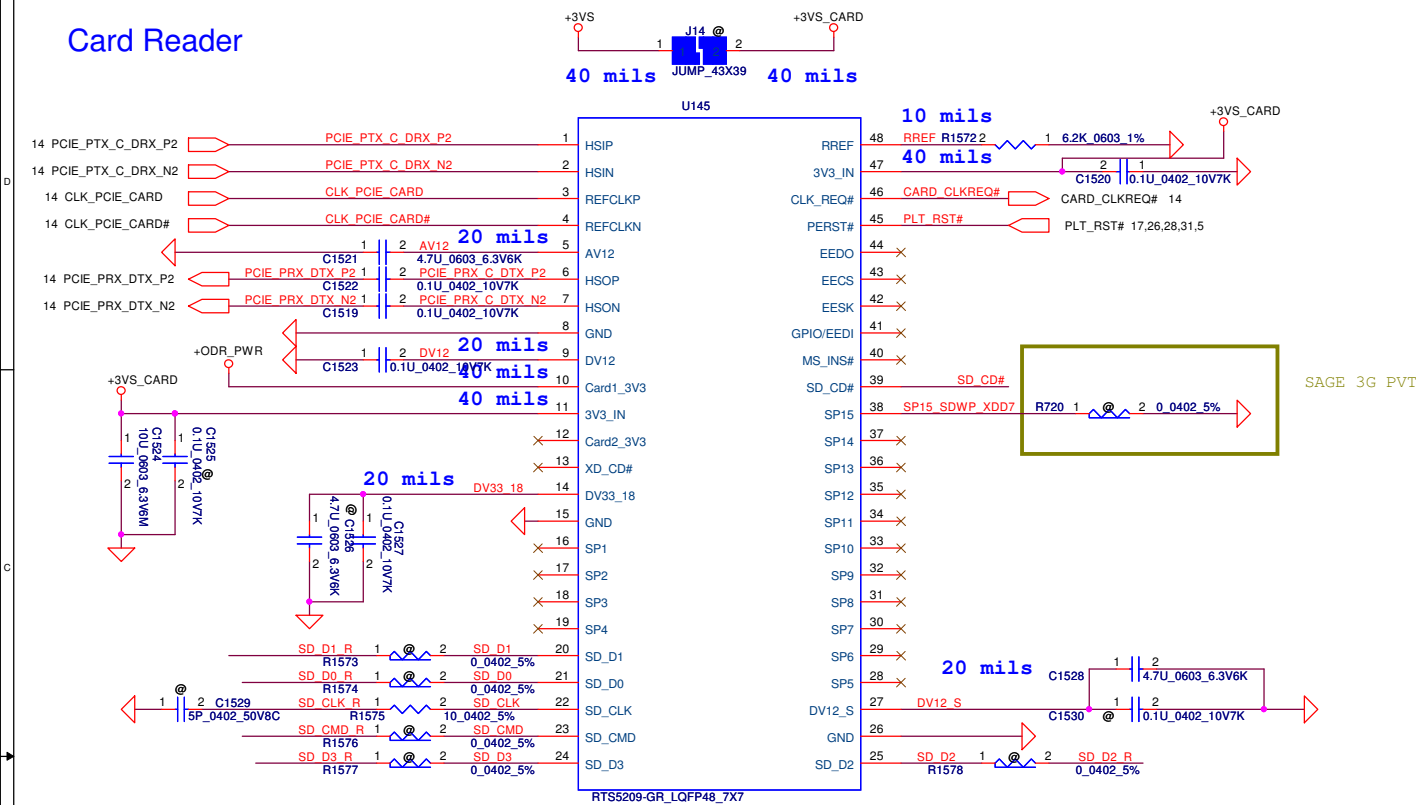


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				V1JB1 M/B LA-A041P Schematic	0.1
				Date: Wednesday, March 13, 2013	Sheet 29 of 52

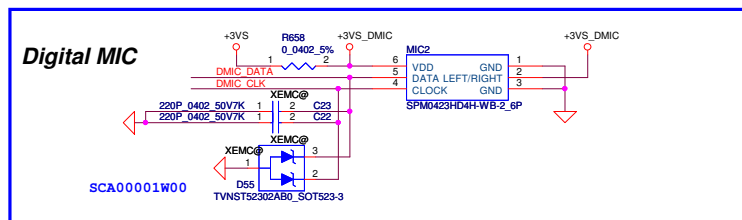
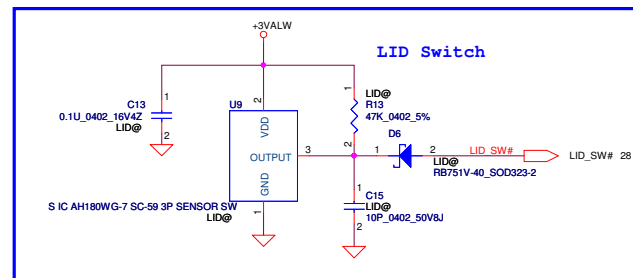
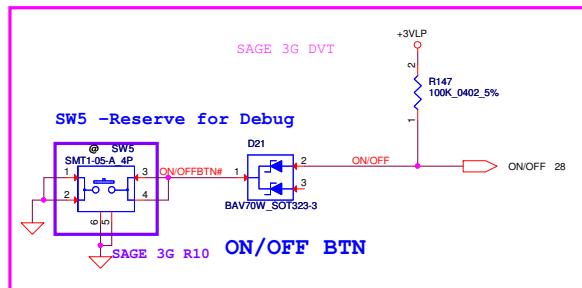
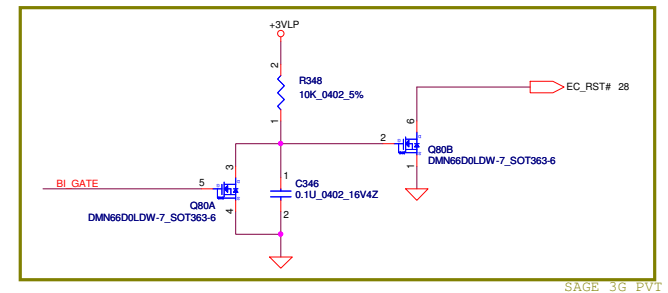
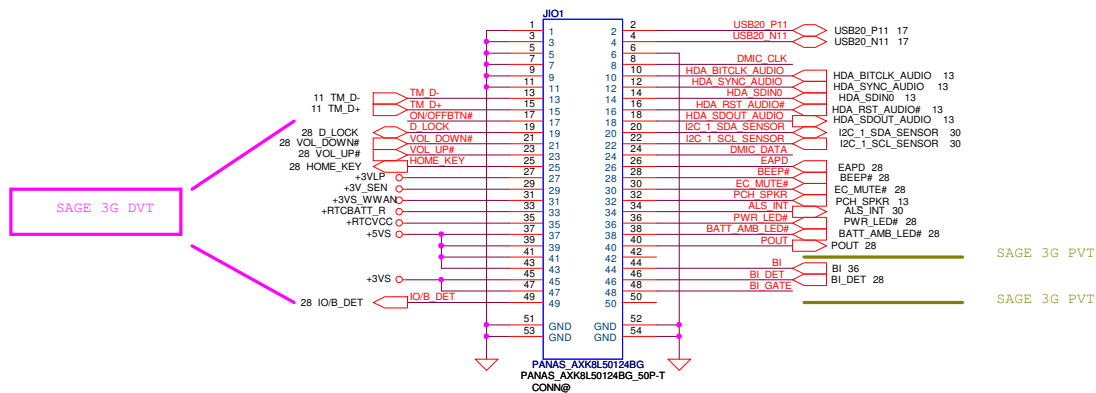


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	SENSOR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPLETE DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size C	Document Number V1J81 M/B LA-A041P Schematic
				Date:	Tuesday, March 26, 2013
				Sheet	30 of 52

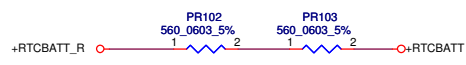
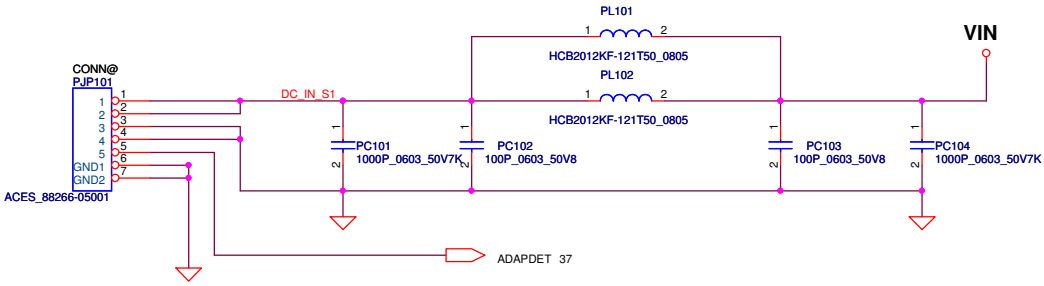
Card Reader



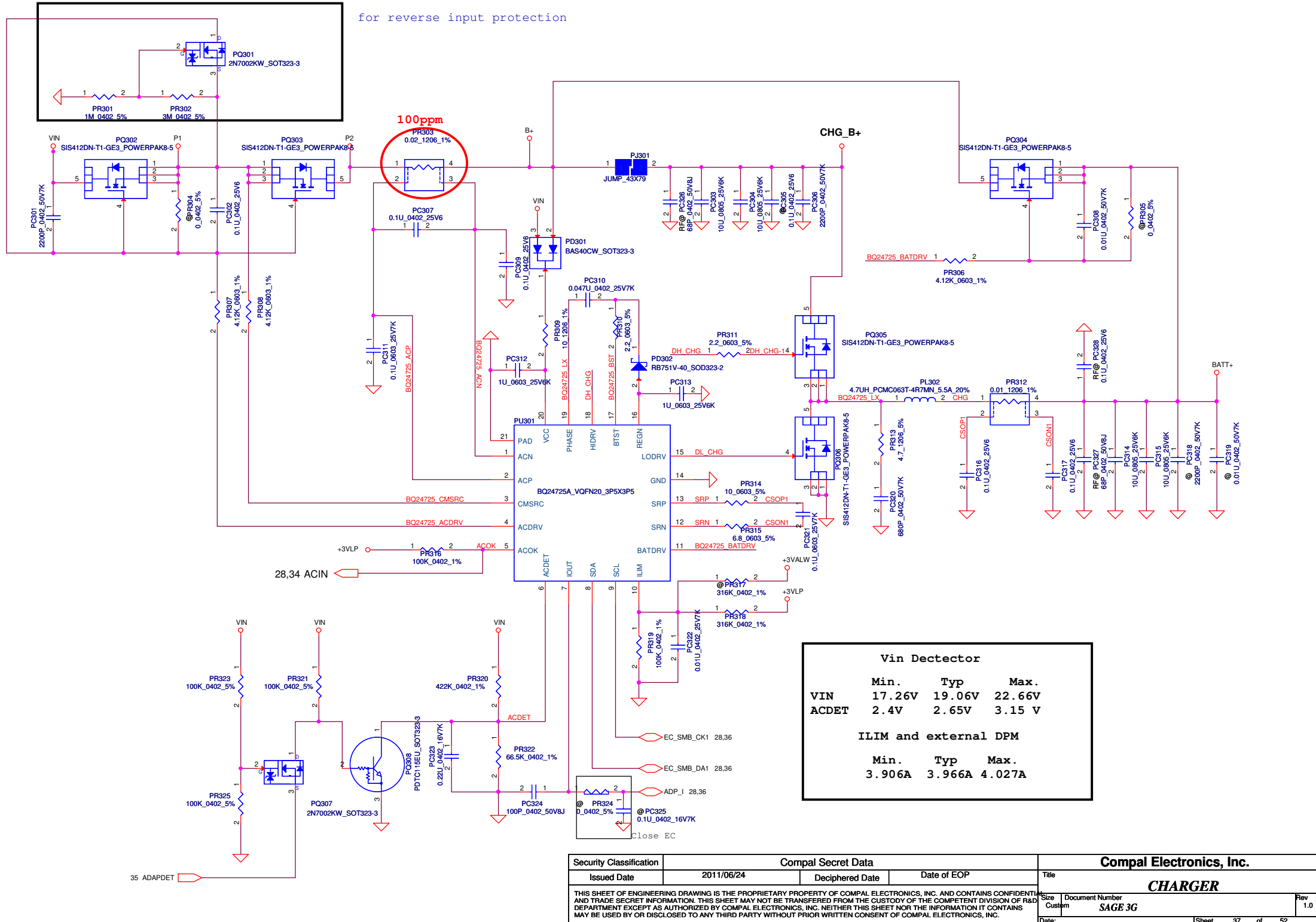
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	Card Reader RTS5209
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Customer	VJ1B1 M/B LA-A041P Schematic
				Date:	Wednesday, March 13, 2013
				Sheet	32 of 52

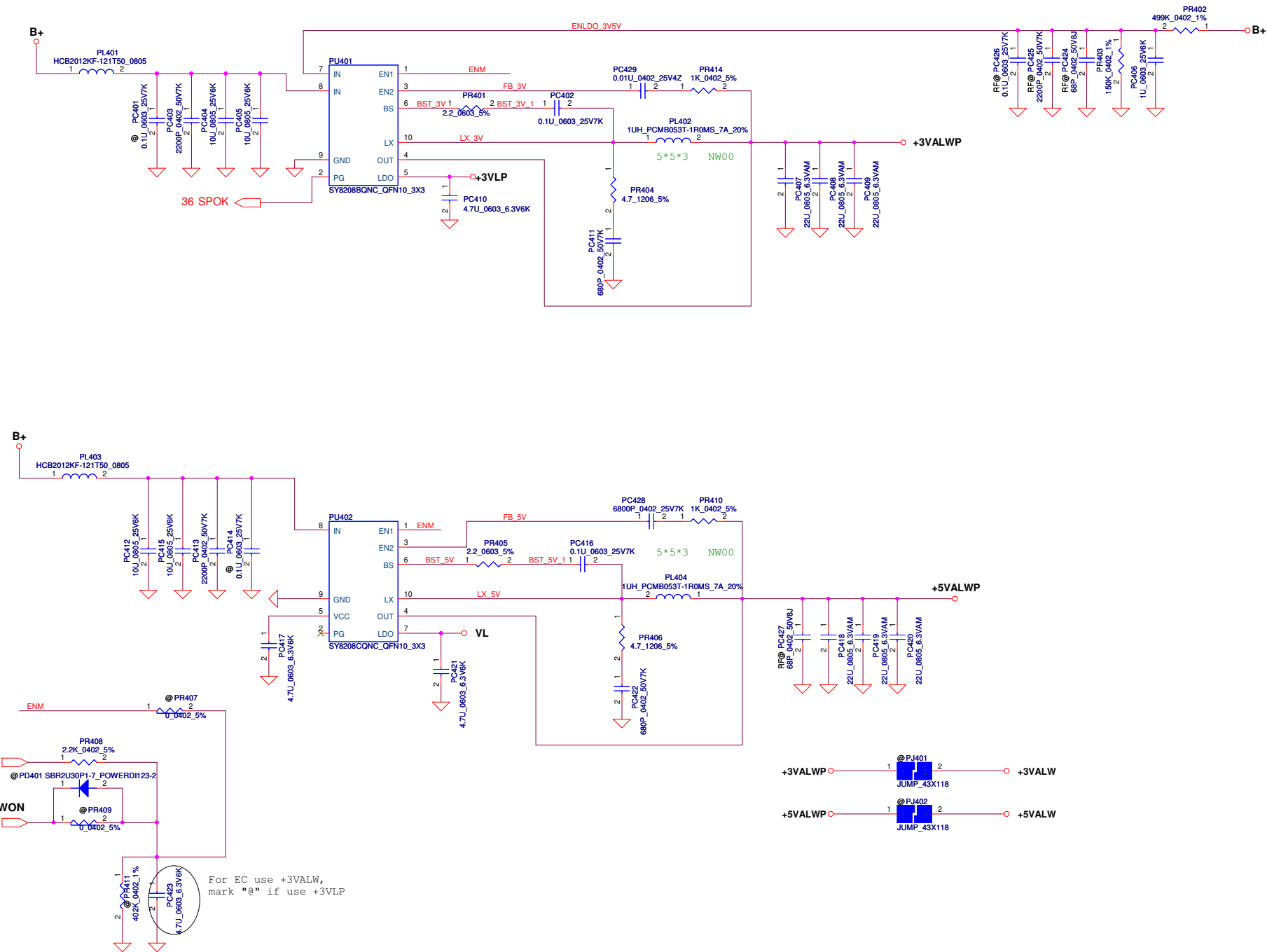


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/1	Deciphered Date	2011/11/1	Title	IO Board (Audio / WIN / RST/ LED)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Customer	V1JB1 M/B LA-A041P Schematic
				Date	Thursday, March 14, 2013
				Sheet	33 of 52
				Rev	0.1



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title	DCIN/PRECHARGE	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	SAGE 3G	1.0
Date:				Sheet 35 of 52		

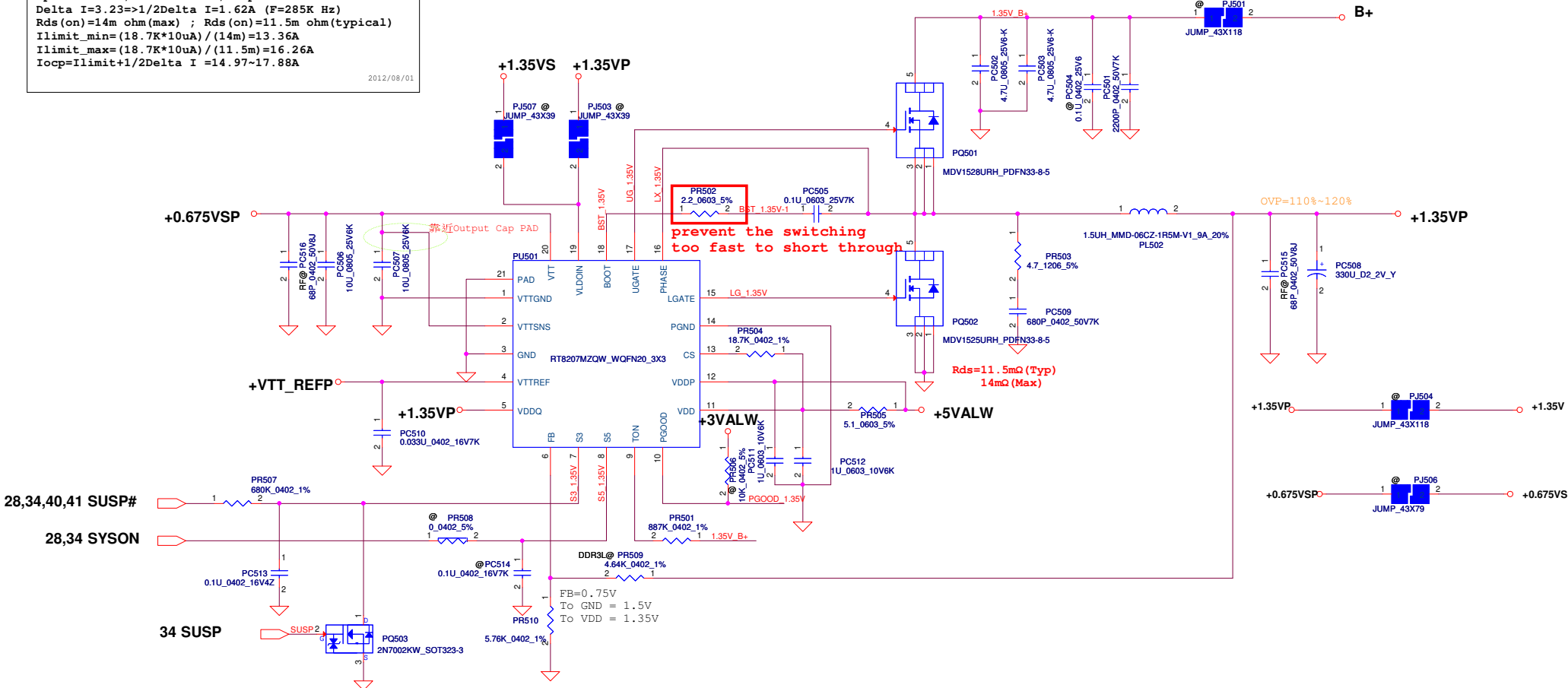




Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/24		Deciphered Date		Date of EOP		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size		Document Number		Rev		1.0	
				Custom		SAGE 3G		Date:		Sheet 38 of 52	

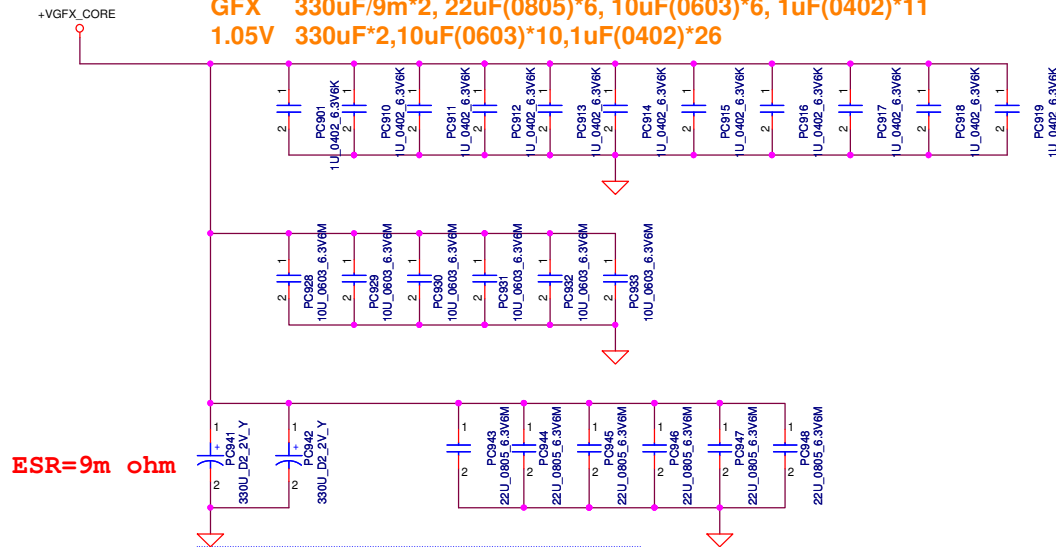
$I_{peak}=12.2A$; $I_{max}=8.54A$; $I_{ocp}=14.64A$
 $\Delta I=3.23 \Rightarrow 1/2\Delta I=1.62A$ ($F=285K$ Hz)
 $R_{ds(on)}=14m\ \Omega$ (max) ; $R_{ds(on)}=11.5m\ \Omega$ (typical)
 $I_{limit_min}=(18.7K*10uA)/(14m)=13.36A$
 $I_{limit_max}=(18.7K*10uA)/(11.5m)=16.26A$
 $I_{ocp}=I_{limit}+1/2\Delta I=14.97\sim 17.88A$

2012/08/01



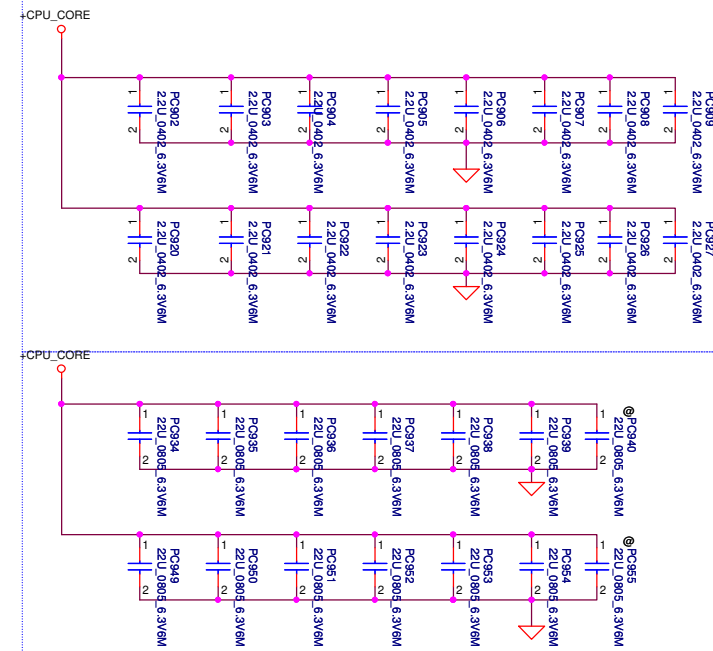
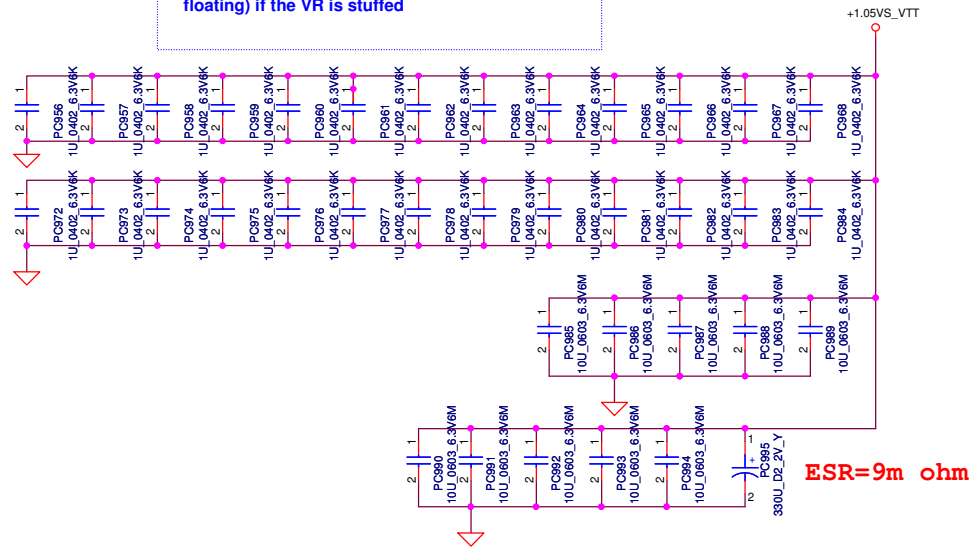
Note: S3 - sleep ; S5 - power off

PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GfX3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFX 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26



Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



For BOT side

For TOP side

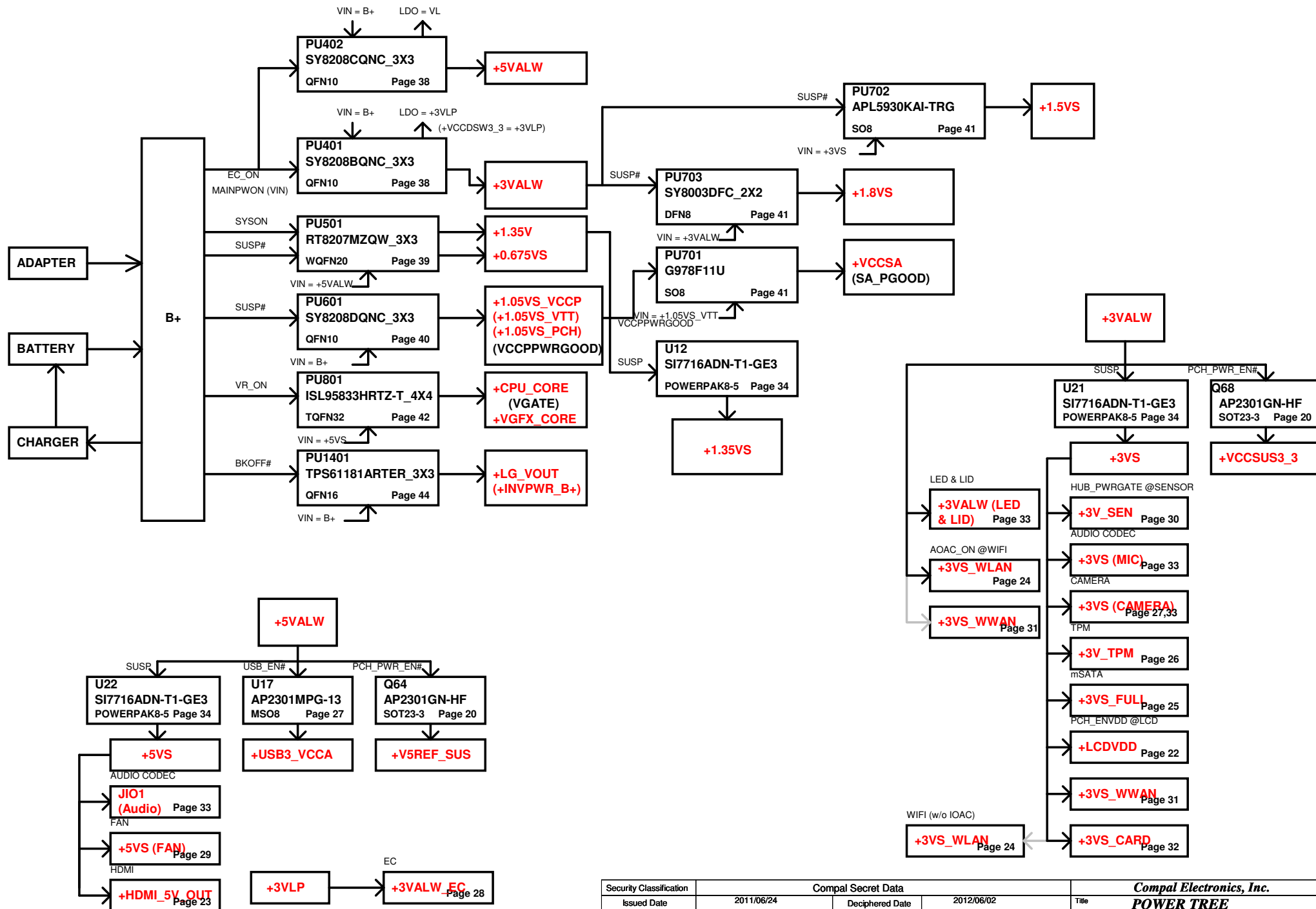
Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2011/06/24		Deciphered Date		Date of EOP		Title							
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								CPU CORE CAP							
								Size		Document Number				Rev	
								Custom		SAGE 3G				1.0	
								Date:						Sheet 43 of 52	

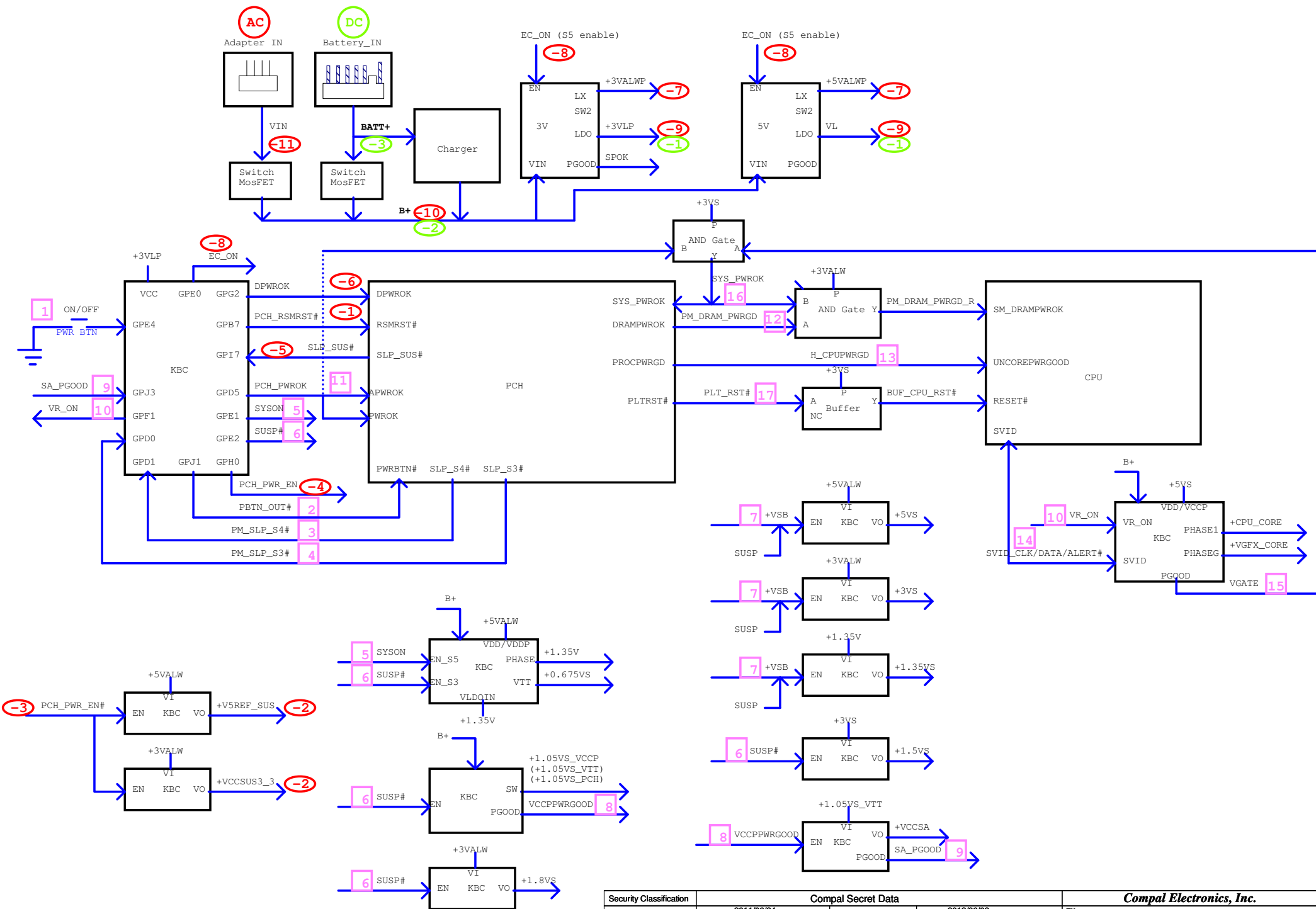
Version change list (P.I.R. List)

Page 1 of 2
for PWR

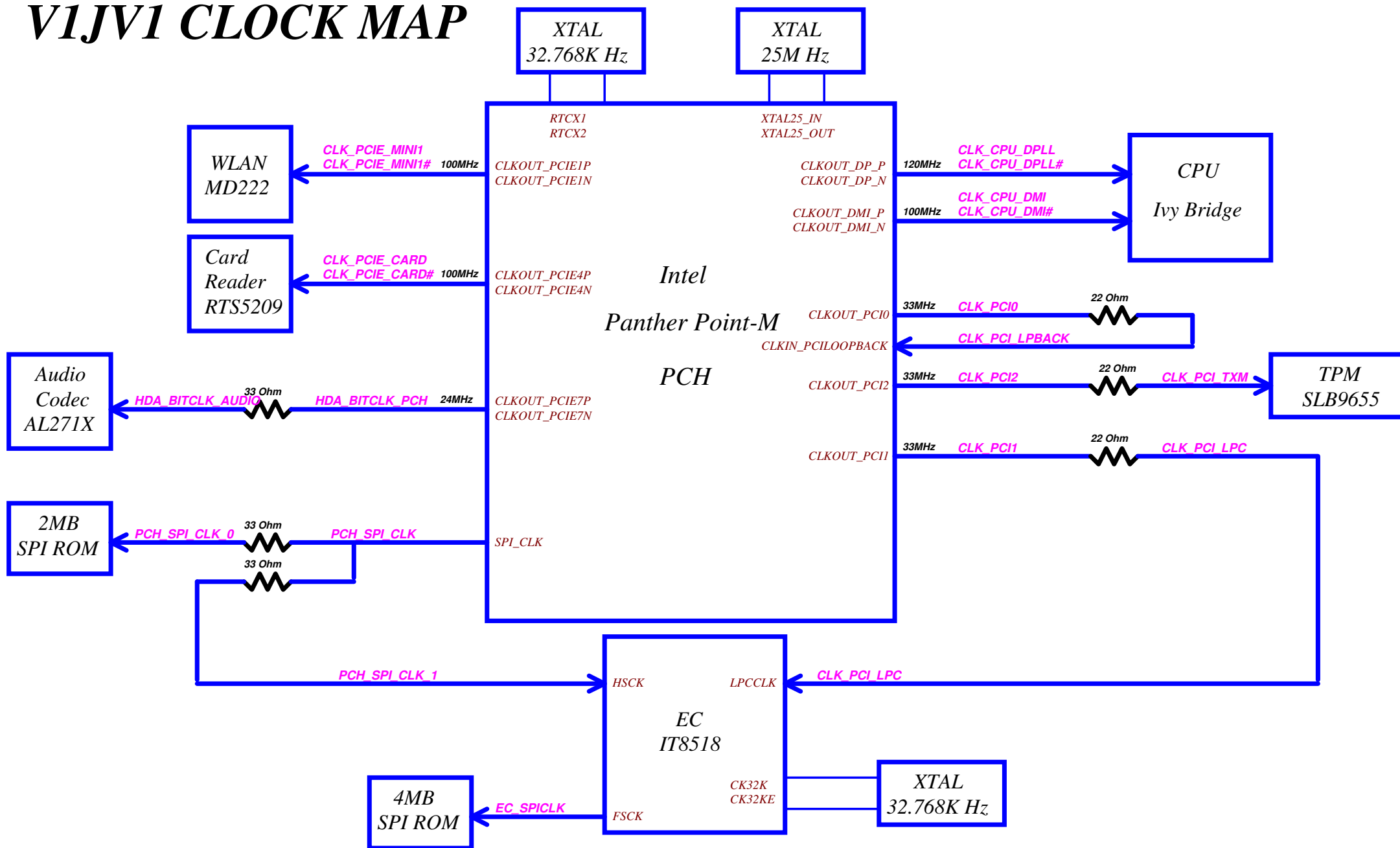
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design Change.	Design Change of IC Application.	0.2	38	Add @PR410.@PR414 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC429 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC428 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR412.@PR413.PR415 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/13	DVT
2	Design Change.	Design Change of IC Application.	0.2	44	Delete PC1413.	2012/12/13	DVT
3	Add Adapter Detection Circuit.	Design Change of DC Jack Application.	0.2	35 37	Add PR325 to SD028000080(S RES 1/16W 0 +-5% 0402) Add PR321.PR323 to SD028100380(S RES 1/16W 100K +-5% 0402) Add PQ307 to SB201440000(S TR PDTA144EU PNP SOT323) Add PQ308 to SB301150200(S TR PDTA115EU NPN SOT323)	2012/12/13	DVT
4	Design Change.	Design Change of IC Application.	0.2	42	Change PC831 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) Change PC832 to SE071560J80(S CER CAP 56P 50V J NPO 0402)	2012/12/24	DVT
5	Change Component Part Number.	Factory lack of material.	0.2	44	Change PL1401 to SH000006J80 (S COIL 4.7UH +-20% PCMC063T-4R7MN 5.5A)	2012/12/24	DVT
6	Change Component Part Number.	Factory lack of material.	0.2	42	Change PC841 to SGA00007I00 (S POLY C 33U 25V M D2 ESR60M TQC H1.9)	2012/12/26	DVT
7	Change Component Part Number.	X1 Code.	0.2	44	Change PD1402 to SCS00005Y00 (S SCH DIO SBR3U40P1-7 POWERDII123-2)	2012/12/26	DVT
8	Design Change.	Design Change of IC Application.	0.3	38	Delete PR412.PR413.PR415.	2012/01/29	PVT
9	Design Change.	Design Change of IC Application.	0.3	38	Change @PR410.@PR414.@PC428.@PC429 to PR410.PR414.PC428.PC429.	2012/01/29	PVT
10	Design Change.	Design Change of IC Application.	0.3	38	Change PC428 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) Change PC429 to SE072103280(S CER CAP .01U 25V Z Y5V 0402)	2013/02/22	PVT
11	Design Change.	Design Change of Adapter Detection.	0.4	37	Change PQ307 to SB000009Q80(S TR 2N7002KW 1N SOT323-3) Add PR325 to SD028100380(S RES 1/16W 100K +-5% 0402)	2013/02/23	Pre MP

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (PWR)	
				Document Number	Rev
				EG51_HX M/B LA-9491P Schematics	1.0
Date:				Sheet	45 of 52



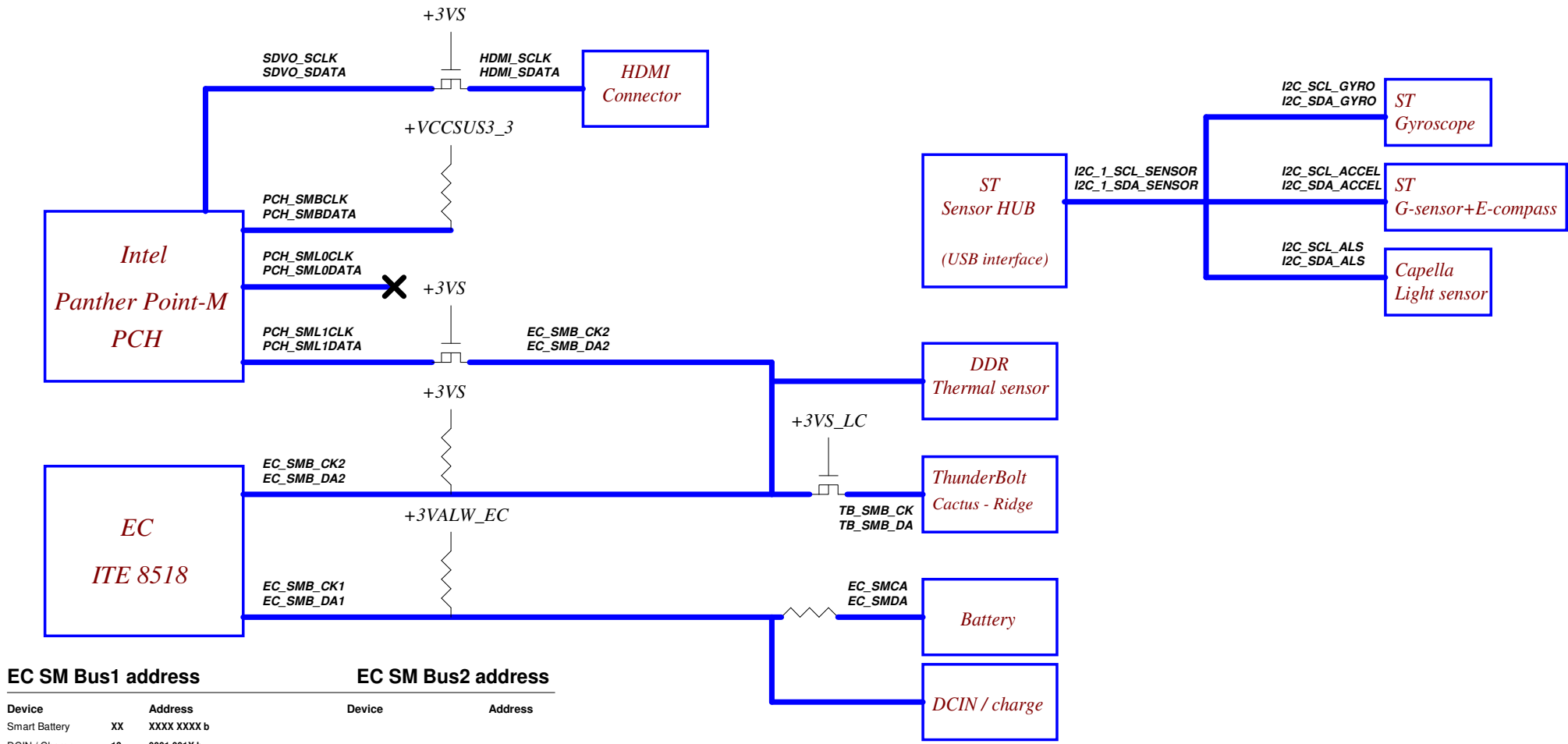


V1JV1 CLOCK MAP

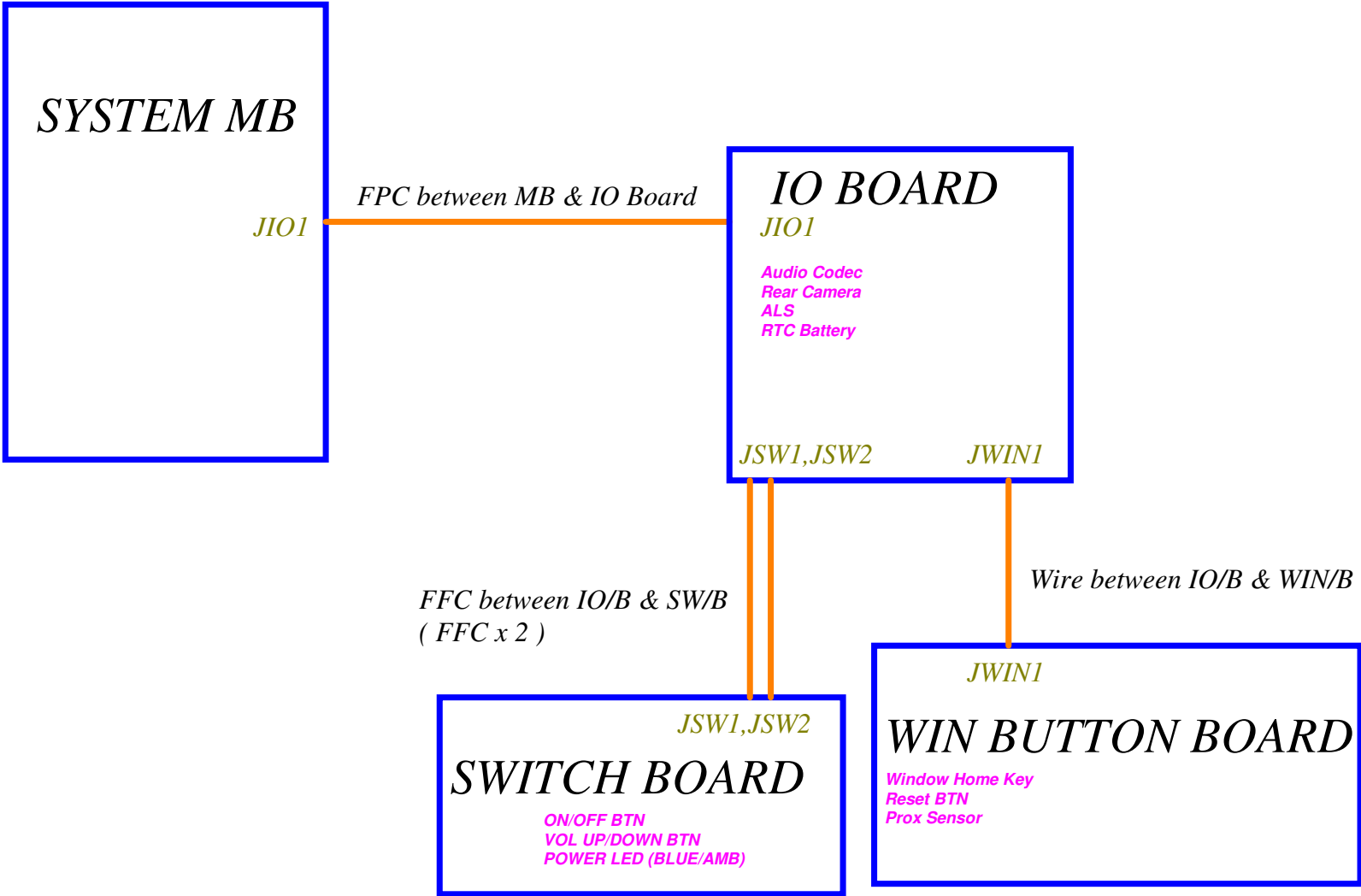


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	CLOCK MAP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				V1JB1 M/B LA-A041P Schematic	0.1
				Date: Wednesday, March 13, 2013	Sheet 48 of 52

SMBUS Block Diagram



V1JB1 SYSTEM Diagram



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
------	-------	-------	------	------------------	-------------------	----------------------	------

- DVT
01. Add net " IO/B_DET" to detect IO/B
 - Avoid thermal sensor wrong action by remote mode cause system auto shut down
02. Add 3 clips at ext USB area (RF requirement)
03. Move D_LOCK pull up resistor from IO/B to M/B side (Reserve function)
04. Move ON/OFFBTN# circuit from IO/B to M/B side(Sub/B just SW BTN only)
05. Change R960 to 8.2k ohm (Board ID update)
06. Change RP19, RP20 package to R_0402*8 (HDMI signal fine tune requirement)
07. Change C451,C450 BOM structure to XEMC@
08. Delete R78 for Layout components reduce
09. Change SIM Card Connecotor as MOLEX_503960-0694 (ME requirement)
10. Change C548 to 0 ohm resistor (3G power from +3VS, not +3VALW)
11. Base on crystal vender suggest, change C756, C757 to 15pF, C744 & C745 to 12pF
- PVT
01. Add test point at CPU pin B22, A19, B14, A11, B10, B6 (DFB requirement)
02. Modify EC_RST# circuit for Reset Button (Dual Mosfet)
03. Add ODT1, CKE1, CS1# net to DDR for 8Gb DRAMs
04. Remove EC_ON, MAINPWON net from JIO1 (un-used net)
05. Change R960 to 18k ohm (Board ID update)
06. Change R185, R186, R720 to shortpad
07. Change R637 to 33 ohm (3G PWR SEQ)
08. Reserve 0 ohm resistor to GND for sensor PB13 as ST suggestion
09. Remove Screw "H18" (ME outline modify)
10. Unstuff 3G power switch circuit (un-used -> 3G power source tie to +3VS directly)
11. Add 3G@ BOM option for WiFi only sku
12. Change R499, R503, R504 from 10k to 100k for DS5 power consumption
- R10
01. Change RP43 part number from SD302220A00(22 ohm) to SD309220A80 (22 ohm) for Green BOM request
02. Unstuff component of reserve circuit (un-used function) ->
 R503, Q7 (SIM_DET# to EC), R504 (EC_3G_ON_OFF#), R260, R311, R505, C407 (3G Ext. RST#)
03. Change R960 to 33k ohm (Board ID update)
04. Unstuff R485 to avoid leakage to wlan module (3G provide power when S3/DS3)
05. Unstuff SW5 (for test phase only, MP remove)
06. Update PCB PN to R10
07. As source request (cancel vender-Cheng Hann), change below parts~
1. Change L23 PN from SM01000AX00 to SM01000EP00
2. Change L3, L4, L36, L38, L39, L40, L53, L68 PN from SM070001600 to SM070001E00
3. Change L52 PN from SM070001310 to SM070001E00
- R20
01. Add USB switch to 3G USB signals for avoid DS3 leakage
02. Delete Q7, R503 (un-used component)
03. Rename EC_SIM_DET# to EC_3G_PWR_EN# (correct net name to meet actual function)
04. Change EC GPD7 (U53.M12) to EC_3G_USB_ON for 3G USB switch
05. Change R960 to 56k ohm (Board ID update)
06. Update PCB PN to R20

PCB

ZZZ1
LA-A041P MB Rev0: DAA0006P000
LA-A041P MB Rev1: DAA0006P010
LA-A041P MB Rev2: DAA0006P020
LA-A041P REV2
DAA0006P020

WLAN/BT Module

U1
LIONMD222@
PK29S004B00
S_W/L_MOD WCBN3501A W/BT MD222 ABO!
WCBN3501A W/BT MD222

CPU

UCPU1
I33217@
S IC AV8063801058401 SR0N9 L1 1.8G ABO!
SA00005L5C0
AV8063801058401 SR0N9 L1 1.8G ABO!

UCPU1
I53317@
S IC AV8063801058002 SR0N8 L1 1.7G ABO!
SA00005K6B0
AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1
I32365M@
S IC AV8062701313000 SR0U3 J1 1.4G ABO!
SA00005UH40
AV8062701313000 SR0U3 J1 1.4G ABO!

UCPU1
I33227@
S IC AV8063801119500 SR0XF L1 1.9G ABO!
SA00006D990
AV8063801119500 SR0XF L1 1.9G ABO!

UCPU1
I53337@
S IC AV8063801129900 SR0XL L1 1.8G ABO!
SA00006D860
AV8063801129900 SR0XL L1 1.8G ABO!

UCPU1
I32375M@
S IC AV8062701313100 SR0U4 J1 1.5G ABO!
SA00006ED50
AV8062701313100 SR0U4 J1 1.5G ABO!

SAGE 3G

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/06/24		Deciphered Date	
				2012/07/12	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	
				Option Component	
				Size	Document Number
				Custom	V1JB1 M/B LA-A041P Schematic
					Rev 0.1
Date:		Thursday, March 14, 2013		Sheet 52 of 52	